

RAA207700GBM/7701GBM/7702GBM

Synchronous Buck Regulator with Internal Power MOSFETs

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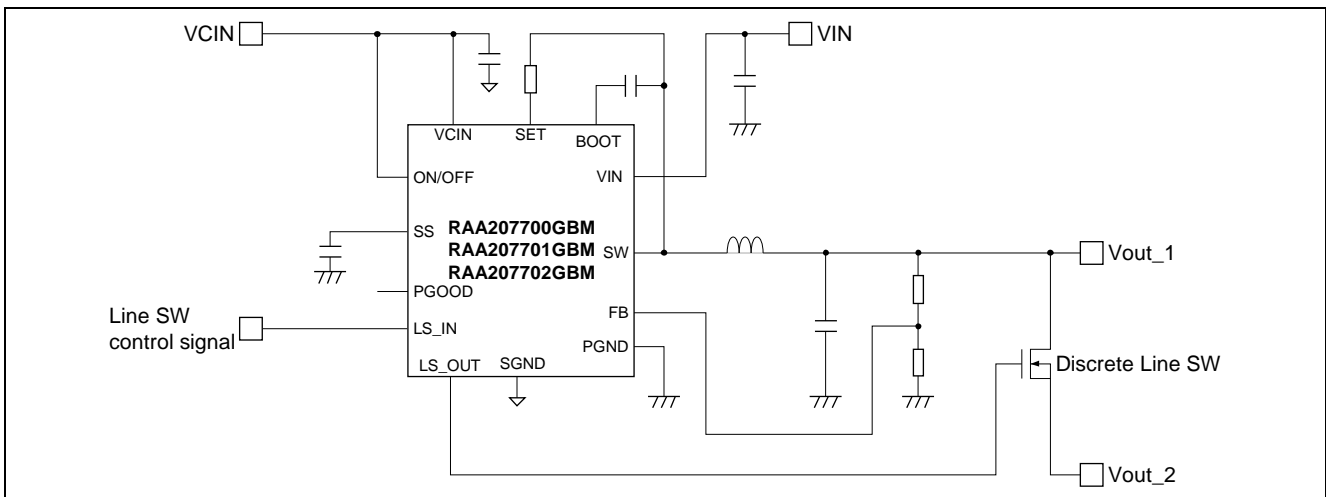
Description

The RAA207700GBM is monolithic synchronous buck regulator with power MOSFETs in extremely small package. The RAA207700GBM delivers high output current by small $R_{ds(on)}$ Power MOSFETs. Constant on time control architecture provides fast transient response, and minimize external components. The RAA207700GBM operates skip mode at light load, it provides high efficiency in all load condition. Three current ability products can be selected.

Features

- Wide input voltage range: 3 V to 16 V
- Output voltage range: 0.8 V to 5 V
- Constant-On-Time control
- Built-in power MOSFETs suitable for PC, Server application
- Very low stand-by current: 0.1 mA (typ.)
- Very low quiescent current :300 mA (typ. at no load)
- Switching frequency: Adjustable up to 2 MHz
- High average output current, up to 15 A (7700GBM), 10 A (7701GBM), 5 A (7702GBM)
- Controllable driver: Remote ON/OFF
- Power Good function
- Over current protection/Over voltage protection/Thermal shutdown function
- Built-in bootstrapping diode
- Soft Start period adjustable
- Enhanced light load mode function for higher efficiency
- High drivability built-in line switch driver for low-loss line switch driving
- Extremely small chip size package with solder bump
- Pb-Free/Halogen-Free

Application Circuit



Pin Arrangement

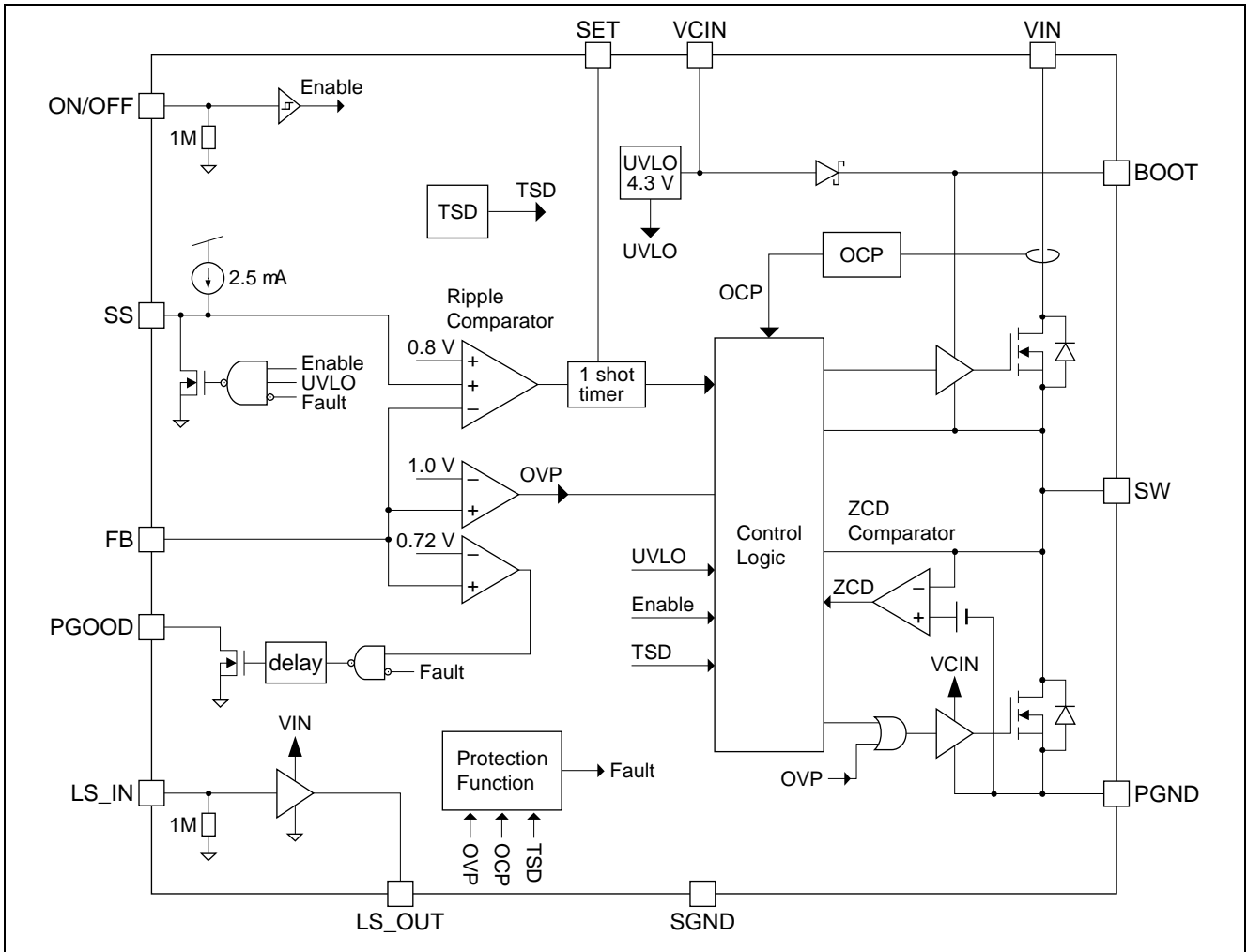


Pin Description

Pin Name	Pin No.	Description	Remarks
VCIN	1A	Controller input voltage (+5 V input)	Controller supply input
SGND	2A	Controller analog GND	Should be connected to PGND on PCB pattern
FB	3A	Feedback voltage input pin	
LS_IN	4A	Line SW driver control pin	
LS_OUT	5A	Line SW driver output pin	
BOOT	1B	Bootstrap voltage pin	To be supplied +5 V through integrated SBD
SET	2B	Constant on time program pin	Tie resistor between SW and SET
PGOOD	3B	Power good indicator pin	Pull low when No Good (open drain output)
SS	4B	Soft start period program pin	Tie capacitor between SS and SGND
ON/OFF	5B	Operation enable pin	Operation stop when "L" signal asserted
VIN	—	Input voltage	
SW	—	Switching node	
PGND	—	Power GND	Should be connected to SGND on PCB pattern

Note: Pin assign of 1A-5A & 1B-5B is common through RAA207700GBM, RAA207701GBM and RAA207702GBM.

Block Diagram



1. Truth table for the ON/OFF pin

ON/OFF Input	Driver Chip Status
"L"	Shutdown (operation STOP)
"Open"	Shutdown (operation STOP)
"H"	Enable (Normal operation)

2. Truth table for Line Switch driver

LS_IN Input	LS_OUT Status
"L"	GND
"Open"	GND
"H"	VIN

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Notes
Input voltage	VIN	-0.3 to +20	V	1
Switch node voltage	SW	20(DC), 23(<10 ns)	V	1
BOOT voltage	VBOOT	25(DC), 28(<10 ns)	V	1, 2
Controller voltage	VCIN	-0.3 to +6	V	1
Input pin voltage (FB, LS_IN)	V _{INPUT}	-0.3 to VCIN +0.3	V	1, 3
ON/OFF voltage	V _{ON/OFF}	-0.3 to VIN	V	1
SET voltage	V _{SET}	-0.3 to VIN	V	1
PGOOD voltage	V _{PGOOD}	-0.3 to VIN	V	1
PGOOD sink current	I _{PGOOD}	+2	mA	4
Operating junction temperature	T _{j-opr}	-40 to +125	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

Notes: 1. Rated voltages are relative to voltages on the SGND and PGND pins.

2. BOOT – VCIN < 20 V

3. VCIN + 0.3 V < 6 V

4. For rated current, (+) indicates inflow to the chip.

Thermal Information

Item	Symbol	Part No.	Value	Unit	Note
Thermal resistance (junction to air when device is mounted on evaluation board)	qj-a	RAA207700GBM	27	°C/W	1
		RAA207701GBM	33		
		RAA207702GBM	39		

Note: 1. Not assured value, just reference for design. Above data is taken using Renesas's reference board.

Recommended Operating Condition

Item	Symbol	Ratings	Unit	Remarks
Input voltage	VIN	3 to 16	V	
Controller voltage	VCIN	4.5 to 5.5	V	
Continuous output current	I _{OUT}	0 to 15	A	15 A: RAA207700GBM 10 A: RAA207701GBM 5 A: RAA207702GBM
		0 to 10		
		0 to 5		

Electrical Characteristics

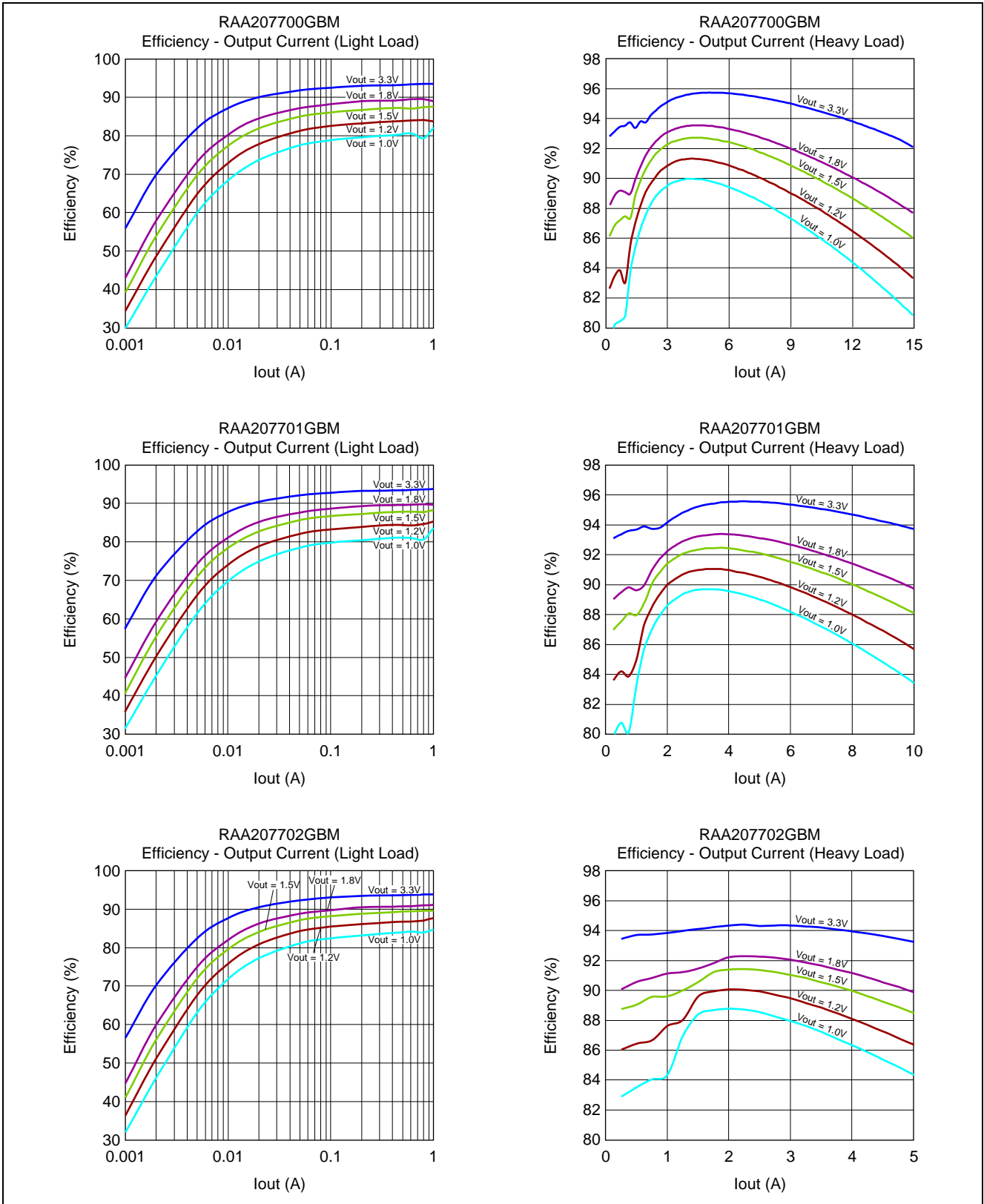
(Ta = 25°C, VCIN = 5 V, VIN = 12 V, unless otherwise specified)

	Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	VCIN start threshold	VH	—	4.3	4.5	V	
	VCIN shutdown threshold in CCM	VLCCM	3.6	3.8	—	V	
	VCIN shutdown threshold in ELL mode	VLDCM	—	3.0	3.6	V	In ELL mode (DCM, f _{sw} < 100 kHz)
	VCIN operating current (RAA207700GBM)	ICIN	—	40	—	mA	f _{sw} = 1 MHz, Ton = 200 ns
	VCIN operating current (RAA207701GBM)	ICIN	—	35	—	mA	
	VCIN operating current (RAA207702GBM)	ICIN	—	20	—	mA	
	VCIN quiescent current	Iq	—	300	450	mA	Output = no load, ELL mode
	VCIN disable current	ICIN-DISBL	—	0.1	5	mA	ON/OFF = 0 V, LS_IN = 0 V
	VIN disable current	IIN-DISBL	—	0.1	5	mA	ON/OFF = 0 V, LS_IN = 0 V
Remote on/off	Disable level	V _{DISBL}	—	—	0.6	V	3.3 / 5.0 V interface
	Enable level	V _{ENBL}	2.0	—	—	V	3.3 / 5.0 V interface
	Pull-down resistance	R _{DISBL}	0.7	1	1.3	MΩ	ON/OFF = 1 V
Line_SW input	Line SW off level	V _{LSIN_OFF}	—	—	0.6	V	3.3 / 5.0 V interface
	Line SW on level	V _{LSIN_ON}	2.0	—	—	V	3.3 / 5.0 V interface
	Pull-down resistance	R _{LS_IN}	0.7	1	1.3	MΩ	LS_IN = 1 V
Line_SW output	Line SW on output voltage	V _{LSW_ON}	VIN-0.5	VIN	—	V	LS_IN = 5 V
	Line SW off output voltage	V _{LSW_OFF}	—	—	0.1	V	LS_IN = 0 V
	Line SW on source current	I _{LSW_SOURCE}	—	25	—	mA	VIN = 12 V, LS_IN = 5 V
	Line SW off sink current	I _{LSW_SINK}	—	25	—	mA	VIN = 12 V, LS_IN = 0 V
	Line SW on propagation delay	T _{PLSWON}	—	300	—	ns	LSIN to LSOUT rising
	Line SW off propagation delay	T _{PLSWOFF}	—	300	—	ns	LSIN to LSOUT falling
	Line SW drive current of VIN	I _{IN-LS}	—	8	20	mA	LS_IN = 5 V
FB	Comparator threshold voltage	V _{FB_COMP}	792	800	808	mV	
	FB input current	I _{FB_IN}	-0.1	0	+0.1	mA	FB = 1 V
1shot timer	High MOSFET on pulse width	P _W	170	210	250	ns	VIN = 12 V, Rset = 30 kW ^{*1}
	High MOSFET minimum on pulse width	P _{MIN_ON}	—	70	—	ns	
	High MOSFET minimum off pulse	P _{MIN_OFF}	—	50	—	ns	
Power good indicator	Rising threshold on FB	V _{PG_rise}	0.67	0.72	0.77	V	
	Power good falling hysteresis	dV _{PG}	—	50	—	mV	
	Power good resistance	R _{PG}	0.25	0.5	1	kΩ	FB = 0 V
Soft start	Soft start bias current	I _{SS}	1.8	2.5	3.3	mA	
Over voltage protection	OVP trip voltage on FB	V _{OVP}	0.95	1.00	1.05	V	
Over current protection	OCP trip current (RAA207700GBM)	I _{OCP}	16.0	20.0	24.0	A	Fixed internally, inductor peak current ^{*1}
	OCP trip current (RAA207701GBM)	I _{OCP}	11.5	14.0	17.0	A	Fixed internally, inductor peak current ^{*1}
	OCP trip current (RAA207702GBM)	I _{OCP}	6.4	8.0	9.6	A	Fixed internally, inductor peak current ^{*1}
Over temperature protection	TSD trip temperature	T _{TSD}	130	150	—	°C	^{*1}
	Temperature hysteresis	T _{hys}	—	15	—	°C	^{*1}

Note: ^{*1} Not directly tested. Assured by related characteristics test.

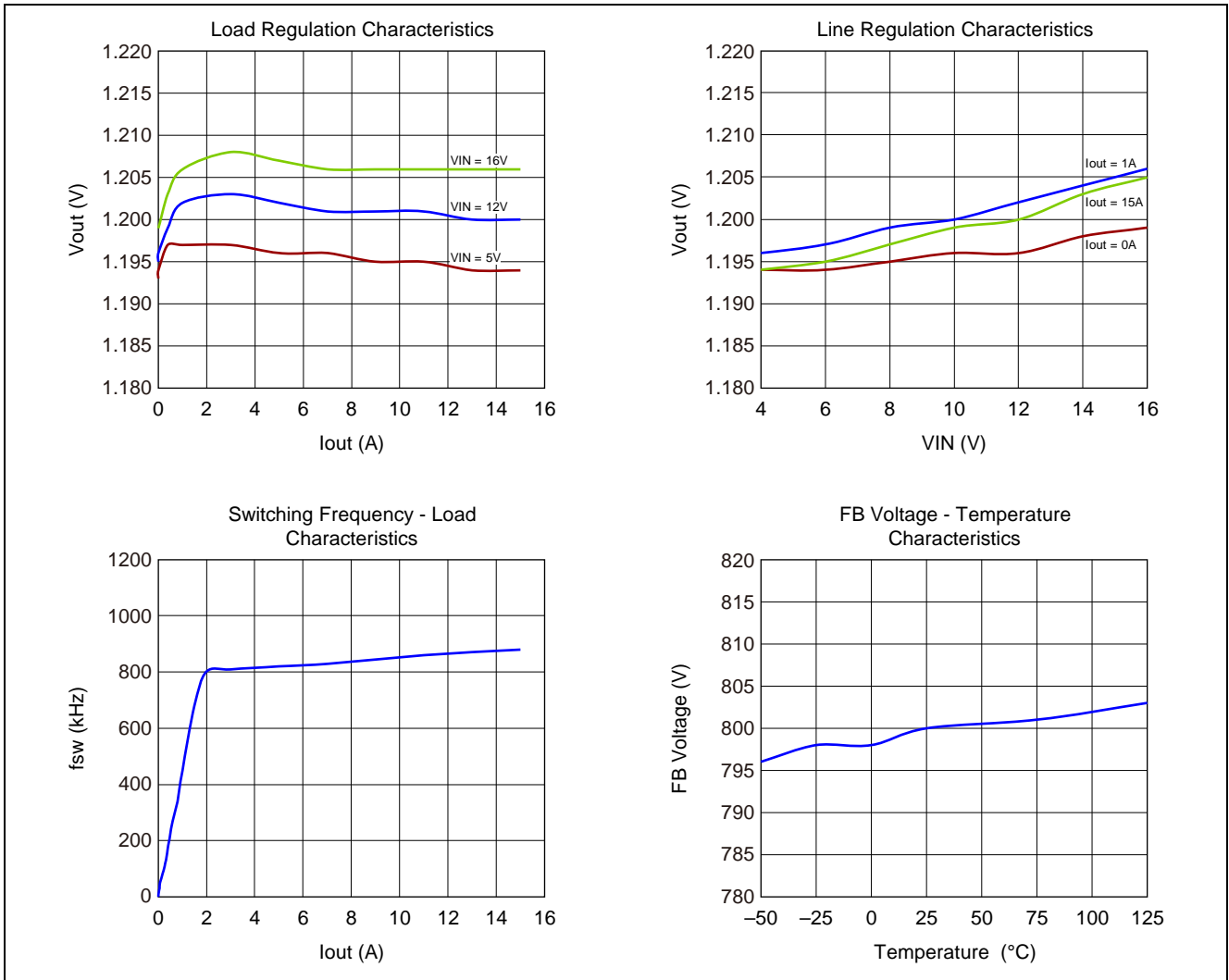
Efficiency Performance

(VCIN = 5 V, VIN = 12 V, L = 1 mH, fsw = 500 kHz (at CCM) no airflow, unless otherwise specified)



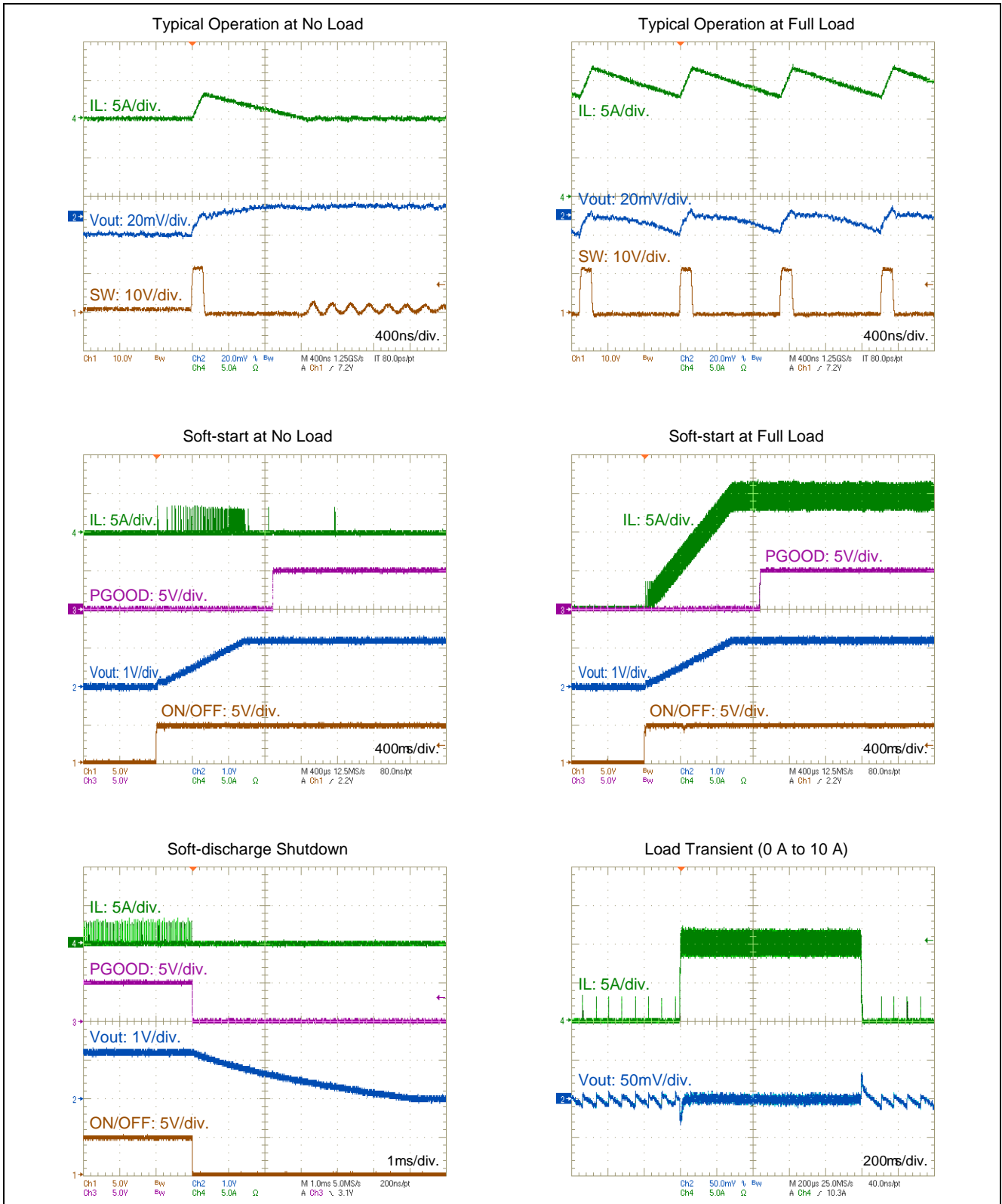
Operating Performance

(RAA207700GBM, $V_{CIN} = 5\text{ V}$, $V_{IN} = 12\text{ V}$, $V_{out} = 1.2\text{ V}$, $L = 0.42\text{ mH}$, $C_{out} = 5 \cdot 47\text{ nF}$, $t_{on} = 130\text{ ns}$, unless otherwise specified)



Operating Waveform

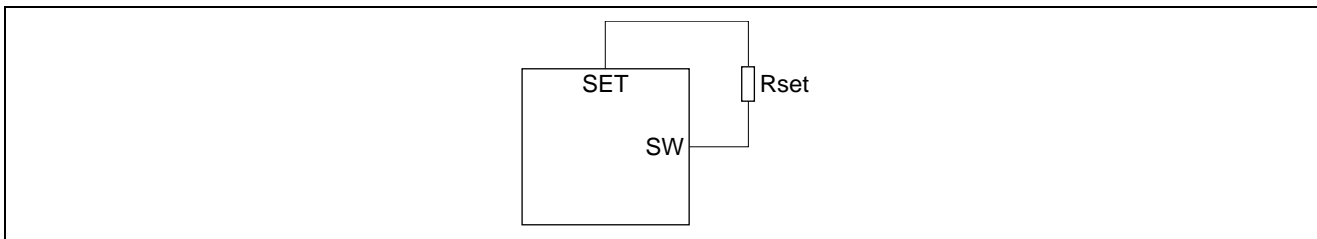
(RAA207700GBM, $V_{CIN} = 5\text{ V}$, $V_{IN} = 12\text{ V}$, $V_{out} = 1.2\text{ V}$, $L = 0.42\text{ mH}$, $C_{out} = 5 \cdot 47\text{ nF}$, $t_{on} = 130\text{ ns}$, unless otherwise specified)



Description of Operation

The RAA207700GBM operates as voltage-ripple based constant on time control architecture. Converter output is controlled by output voltage ripple which is determined by inductor ripple current and ESR & ESL of output capacitor. Each switching cycle starts High-side MOSFET turn on which time is decided by 1 shot timer. After High-side MOSFET turns off, Low-side turns on, and it keeps until FB voltage becomes lower than reference voltage. In light load condition, Low-side MOSFET on time is decided by inductor zero current.

Switching Frequency, Constant on Time Setting



Switching Frequency in CCM mode is determined by following equation.

$$\text{Switching Frequency: } (V_{out} / V_{IN}) \cdot (1 / t_{on}) \text{ [Hz]} \quad (1)$$

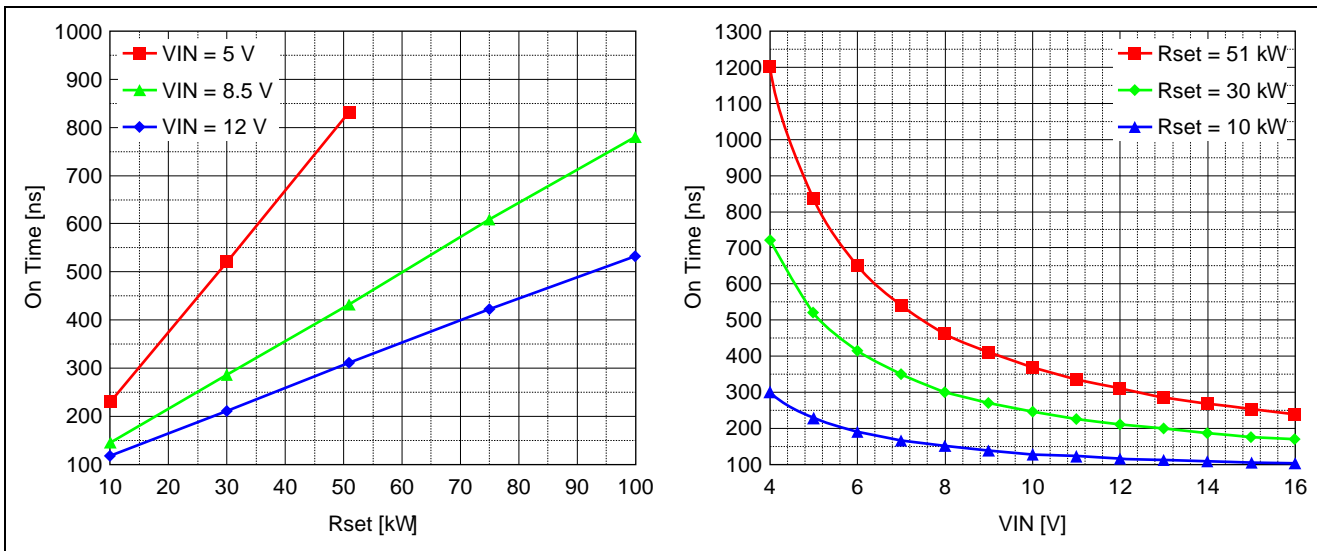
Here, t_{on} is High-side MOSFET on time, and it is determined by following equation.

$$\text{On time pulse: } (50 \text{ pF} \cdot 1 \text{ V} / (V_{IN} - 2.0 \text{ V})) \cdot R_{set} + 60 \text{ ns [s]} \quad (2)$$

From above equation, constant on time is change depend on V_{IN} , so switching frequency is almost constant when V_{IN} change. This architecture is suitable for battery application. From the above equation, R_{set} is calculated by

$$R_{set: } (V_{out} / (V_{IN} \cdot F_{sw}) - 60 \text{ ns}) \cdot (V_{IN} - 2.0 \text{ V}) / (50 \text{ pF} \cdot 1 \text{ V}) \text{ [}\Omega\text{]} \quad (3)$$

Here, F_{sw} is switching frequency.



Minimum on time is 70 ns (typ.), so recommended on time pulse is more than 100 ns. Maximum operating frequency is restricted by minimum on time and minimum off time (50 ns, please see next chapter).

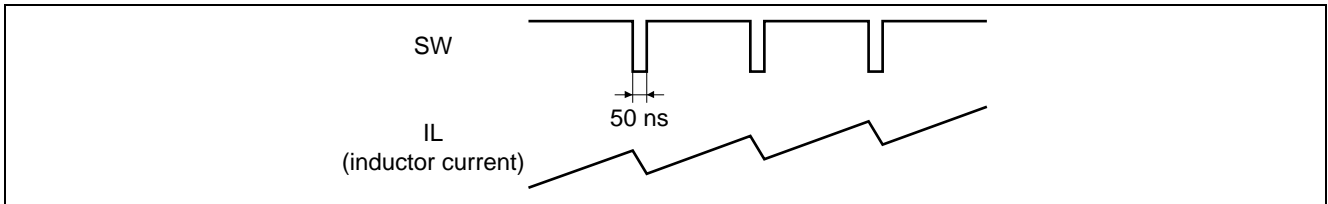
Maximum Duty Cycle Operation

Maximum duty cycle is restricted by following equation.

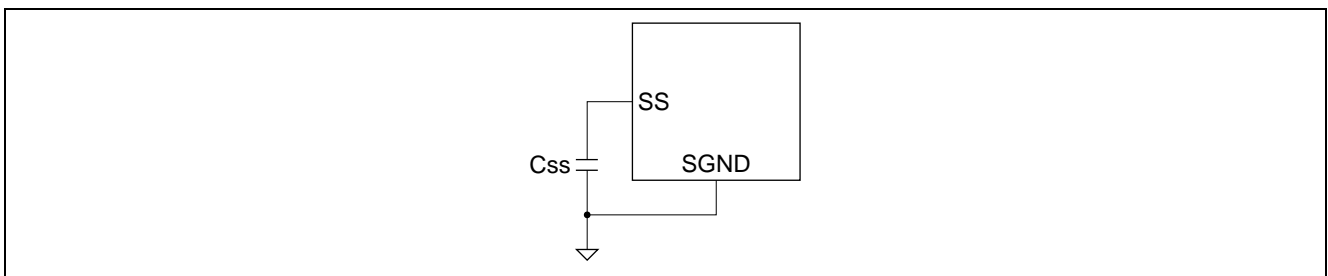
$$\text{Max. duty: } 1 - (50 \text{ ns} \cdot F_{sw}) \frac{1}{4} \quad (4)$$

Here, 50 ns means High-side minimum off time.

If FB voltage does not reach reference voltage after the High-side MOSFET turn on time is expired, Low-side MOSFET turns on 50 ns, and next switching cycle starts. Especially, this condition occurs when output load transient state.



Soft Start



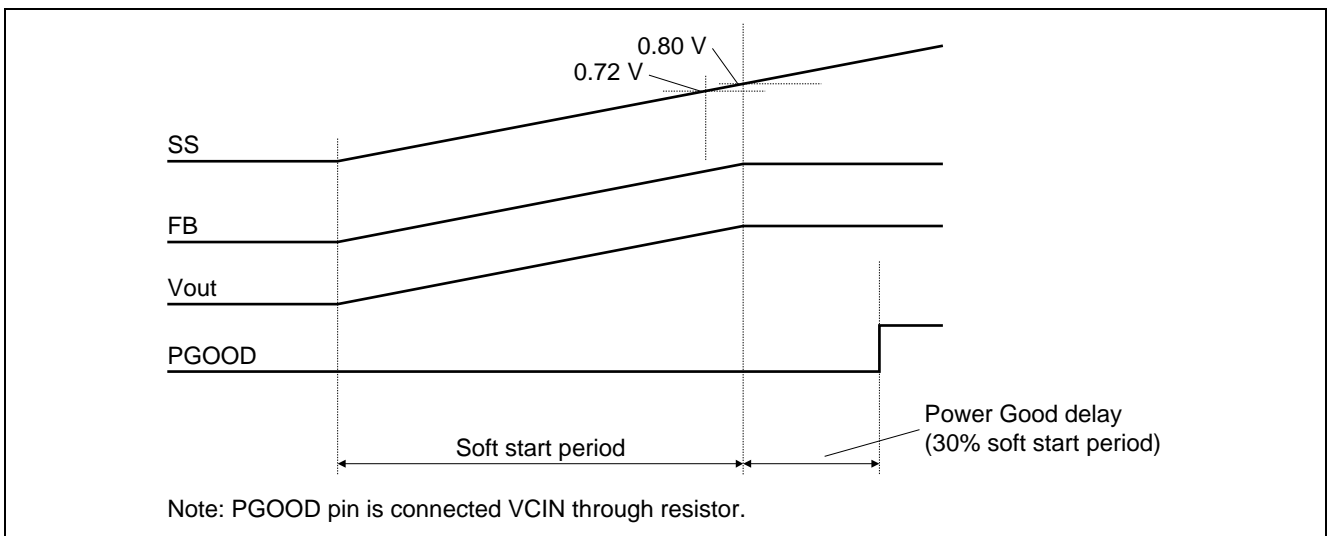
Soft start ramp period is adjustable by external capacitor (C_{SS}) selection. When converter start operating, 2.5 mA current from SS pin charges capacitor between SS and GND. Soft start period is determined by following equation.

$$\text{Soft Start period: } C_{SS} \cdot 0.8 \text{ V} / 2.5 \text{ mA [s]} \frac{1}{4} \quad (5)$$

Here, 0.8 V is internal reference voltage V_{ref}. IC operates diode emulation mode at Soft start period, so it can prevent from reverse current when pre-bias condition. Soft start restarts when Enable signal re-entered, and after OCP, OVP, TSD, UVL release condition.

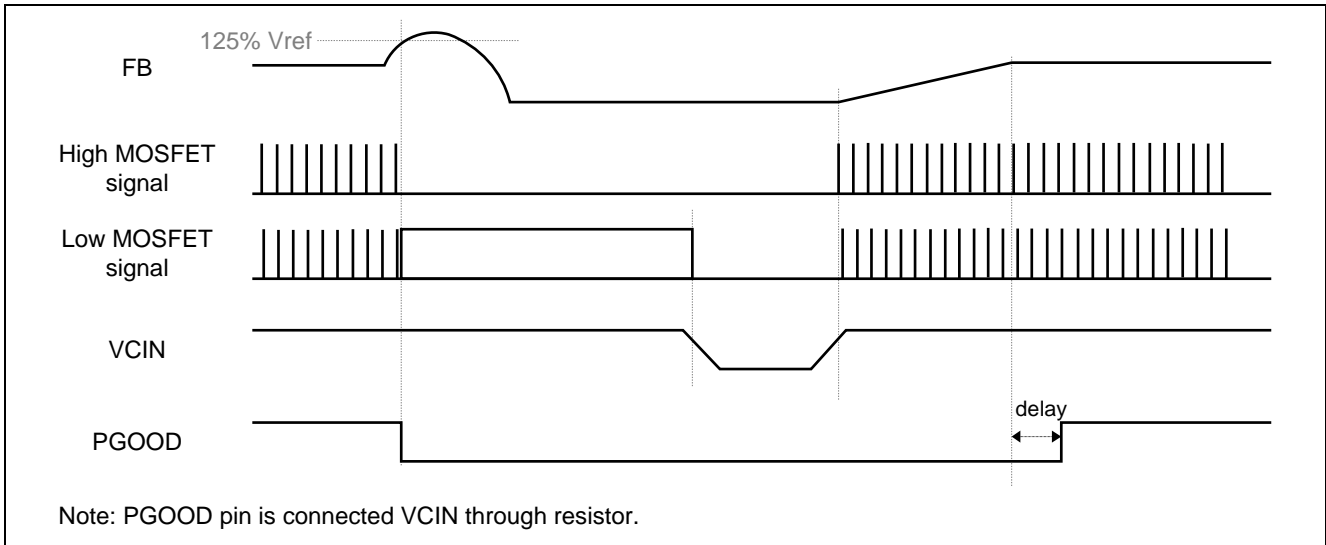
Power Good Indicator

Power good indicator is useful for controlling multi-converter systems for sequential start up and shut down. FB voltage is monitored continuously by power good comparator. The power good comparator compares FB pin and 90% internal reference voltage (0.72 V). When FB reaches reference voltage, PGOOD pin becomes high impedance after internal delay (30% of soft start period). Under the fault condition (UVLO, OVP, OCP, TSD), PGOOD pin is pulled low.



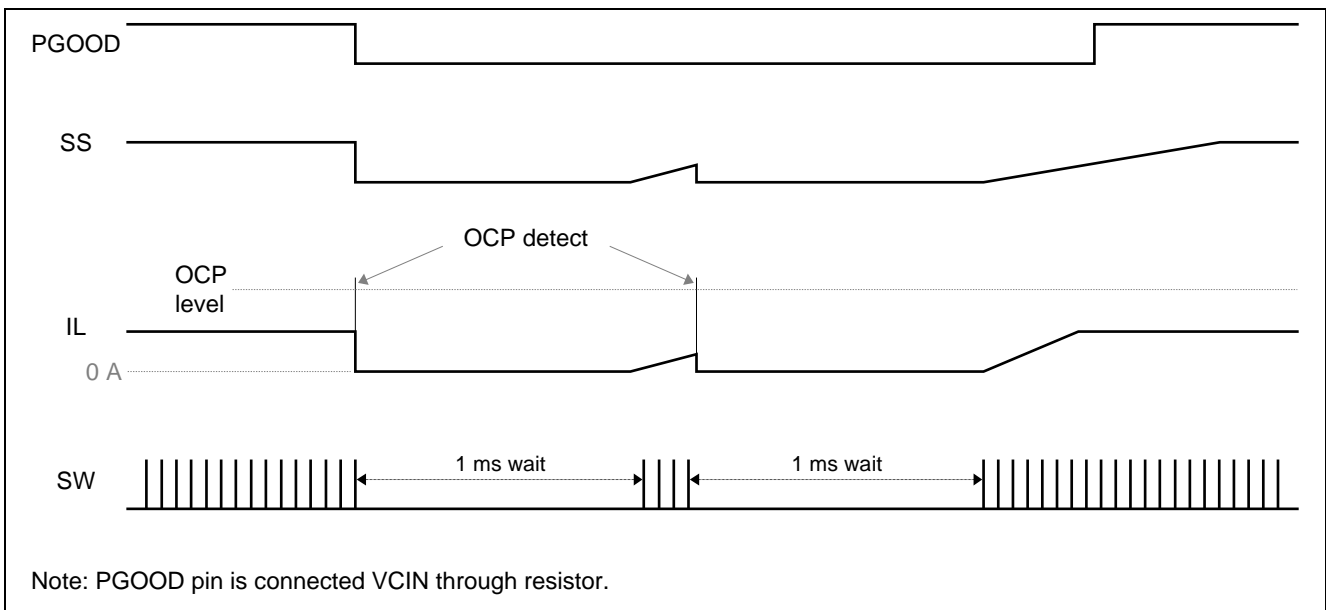
Over Voltage Protection (OVP)

When FB voltage exceeds 125% of reference voltage (1.00 V), switching stops immediately and latched Low-side MOSFET on state in order to pull the output voltage. To leave the OVP condition, VCIN needs to be pulled under the UVLO level, and re-enter the signal.



Over Current Protection (OCP)

OCP detection circuit monitors High-side MOSFET drain-source current. When the current exceeds fixed level four times, IC starts hiccup operation. In the hiccup operation, switching stops and operate 1 ms timer. After 1 ms timer is expired, IC operates again from soft start state. If IC detect OCP in the soft start circuit, hiccup operation start again.



Thermal Shutdown (TSD)

Thermal sensor monitors junction temperature of IC. When junction temperature exceeds 150°C, switching stops. After junction temperature become 135°C, IC restart switching from soft start (Non-latched function).

Enhanced Light Load Function (ELL)

IC operates diode emulation mode in light load condition. To enhance light load efficiency, IC detects light load condition automatically, and operate as Enhanced Light Load mode (ELL). In ELL mode, bias current of IC becomes small, so this function can improve the efficiency.

Line Switch Driver Function

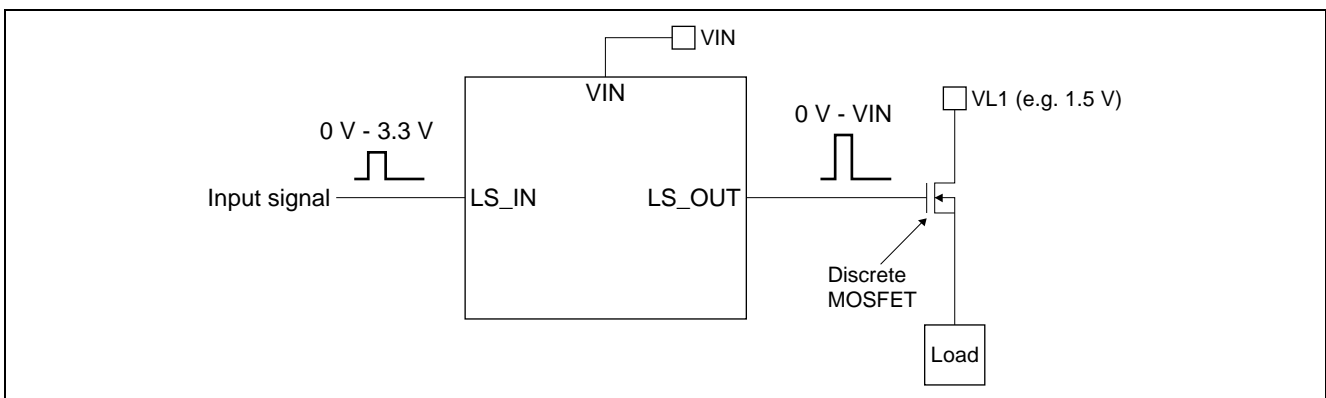
The RAA207700GBM/7701GBM/7702GBM incorporates high drivability built in line switch driver. The line switch driver can drives large gate capacitance MOSFET with low power consumption.

(LS_IN = "H": 8 mA at VIN = 12 V, LS_IN = "L": no power consumption)

Line switch driver operates independent of voltage regulator's state.

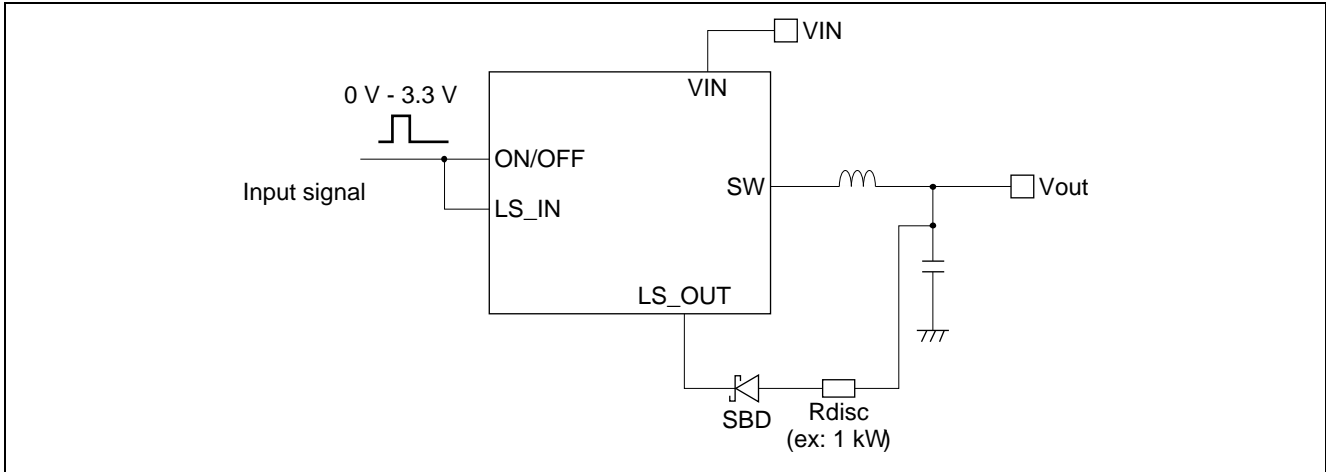
Application Example (1) - Line Switch (Power MOSFET) Driver

Line switch driver function is typically used for power MOSFET drive for power supply control. This function can realize very low power line switch control.



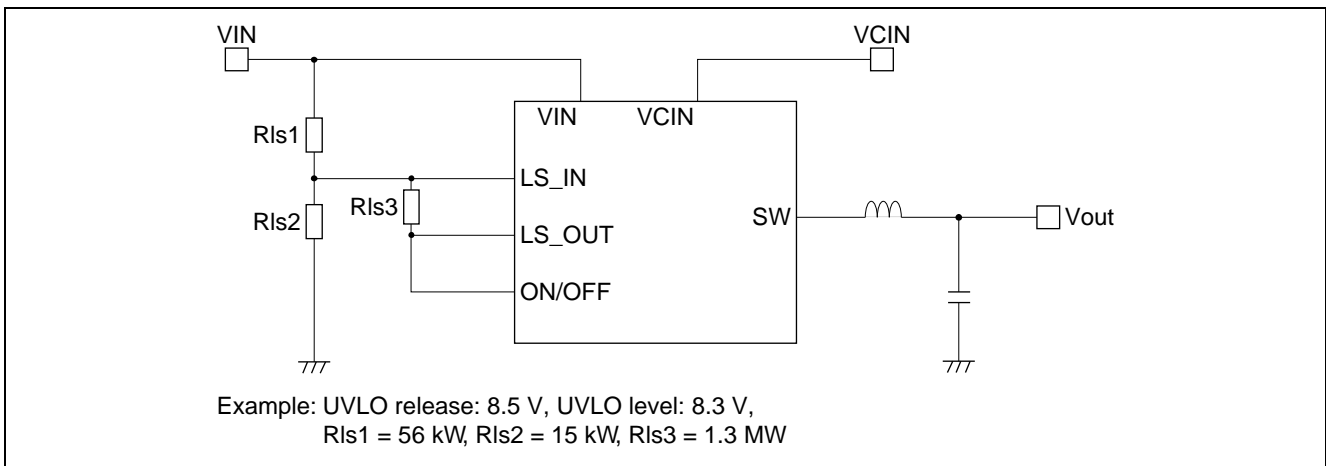
Application Example (2) - Output Voltage Discharge Control

Line switch driver can be used as a fast Vout discharge function when ON/OFF = "L" signal asserted. Wire connection is described below. When "H" signal is asserted to ON/OFF, IC start operating as a voltage regulator, and LS_OUT outputs voltage of VIN. To block current from LS_OUT to Vout, need Schottky Barrier Diode(SBD) or normal Diode that have enough blocking capacity. When ON/OFF signal becomes "L", LS_OUT starts to discharge Vout through SBD. To control discharge time and slew rate, resistance between Vout and LS_OUT is effective.



Application Example (3) - Sequence Free Start-up (Add UVLO Function on VIN Voltage)

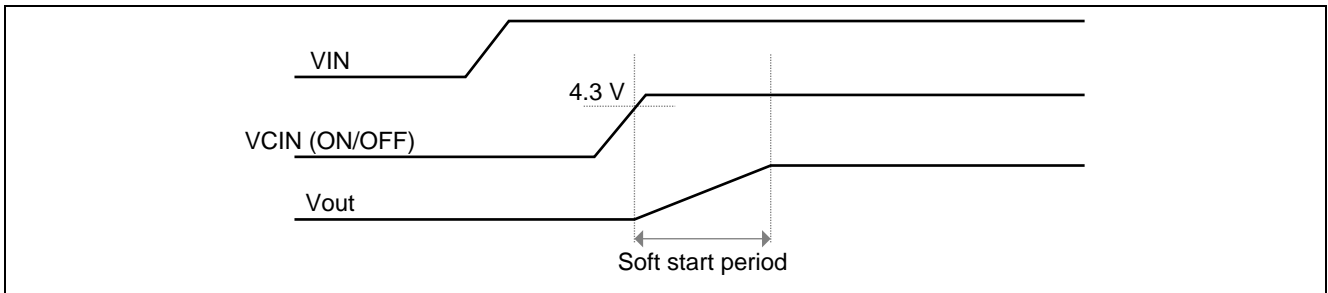
The RAA207700 series does not have UVLO function on VIN, so power on sequence is needed in start-up stage (Please see chapter "power up sequence"). However UVLO function can be add on VIN using line switch driver function. Wire connection is described below. Rls1 and Rls2 are voltage divider of VIN, Rls3 is for hysteresis of UVLO. UVLO level can be adjusted by tuning Rls1, Rls2 and Rls3.



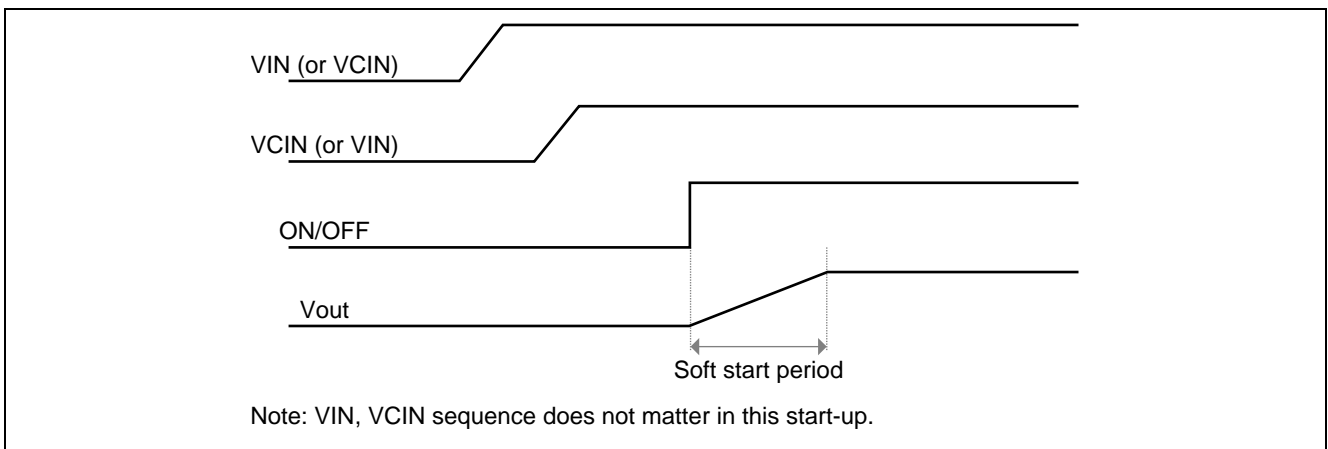
Start-up Sequence

The RAA207700GBM series need specific start-up sequence. Please set start-up sequence from following. IC cannot start-up when "VCIN & ON/OFF rise first, VIN rises secondly" sequence.

(1) VIN to VCIN & ON/OFF (ON/OFF is pulled up to VCIN)

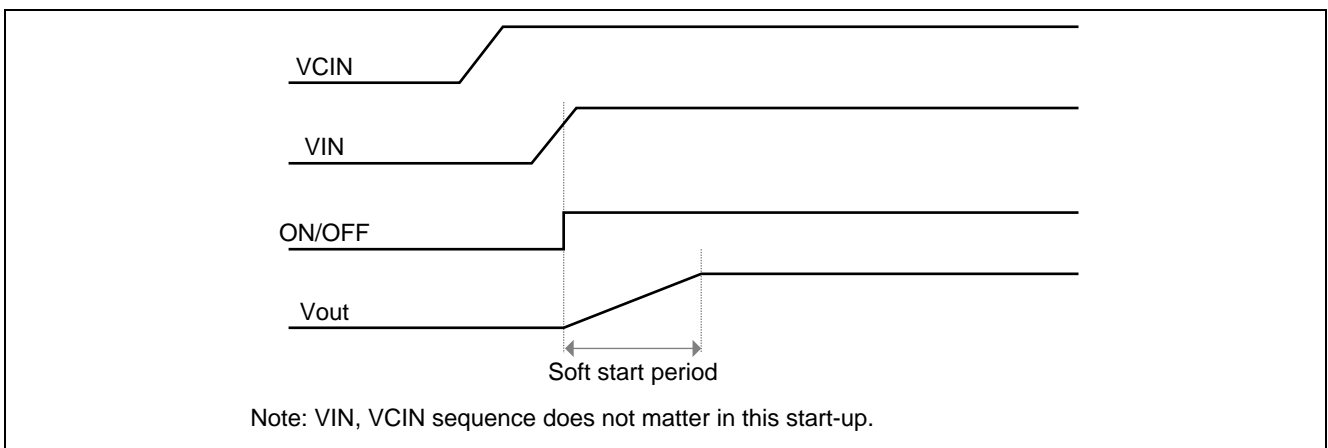


(2) VIN or VCIN to ON/OFF (ON/OFF = "H" asserted after VIN & VCIN rise)



(3) VCIN to VIN (ON/OFF) (from previous chapter, using Line switch driver function)

Please see Line switch driver function(3); sequence free start-up.



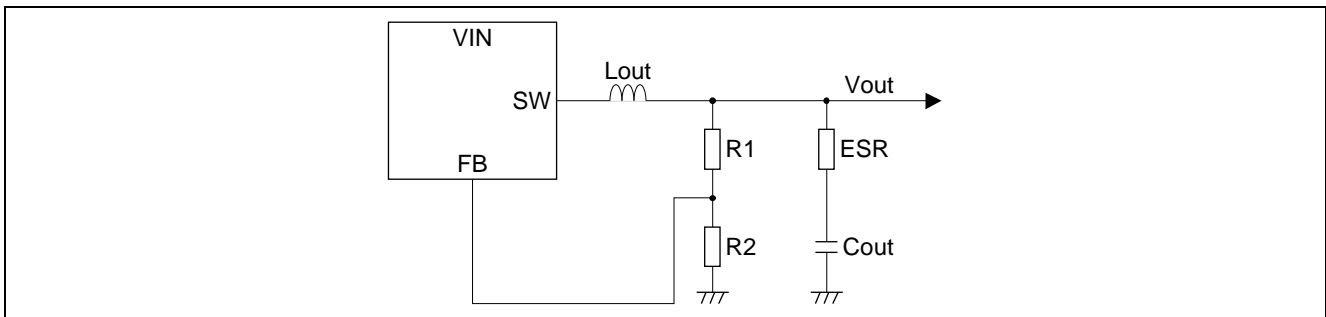
ON/OFF Pin Slew Rate Restriction

When ON/OFF pin is driven by another controller, the slew rate of H to L transition must be higher than -5 V/ms monotonically (must be rapid transition). If the slew rate is lower than -5 V/ms (slow transition), switching noise affect ON/OFF pin input circuit and lead to malfunction in case of heavy load state. Recommended drive impedance of ON/OFF pin is less than $10 \text{ k}\Omega$. If ON/OFF pin is always pulled up to VCIN or VIN via resistance, slew rate is not a matter.



Stability Criteria, Output Voltage Setting for High ESR Output Capacitor

Small output ripple voltage makes control loop unstable in constant on time architecture. Ripple voltage needs to be larger than 15 mV on FB pin. When using high ESR ($>50 \text{ m}\Omega$) capacitor such as Electrolytic capacitor, Polymer aluminum capacitor for output capacitor, ripple voltage on FB pin will be more than 15 mV .



Stability criteria

From loop stability analysis, constant on time control system must satisfy below equation.

$$\text{Stability criteria: } \text{ESR} \cdot \text{Cout} > \text{ton} / 2 \text{ } \frac{1}{4} \text{ (6)}$$

Here, ton is constant on time. If the system cannot satisfy above equation, subharmonic oscillation will occur.

Vout setting

FB comparator compares FB voltage and internal accurate reference voltage (0.8 V). Feedback loop controls FB voltage to match the reference voltage. However, Vout ripple voltage affects FB voltage. So, effective FB pin voltage Vfb will be below. (Here, Vout ripple from bulk capacitance is ignored)

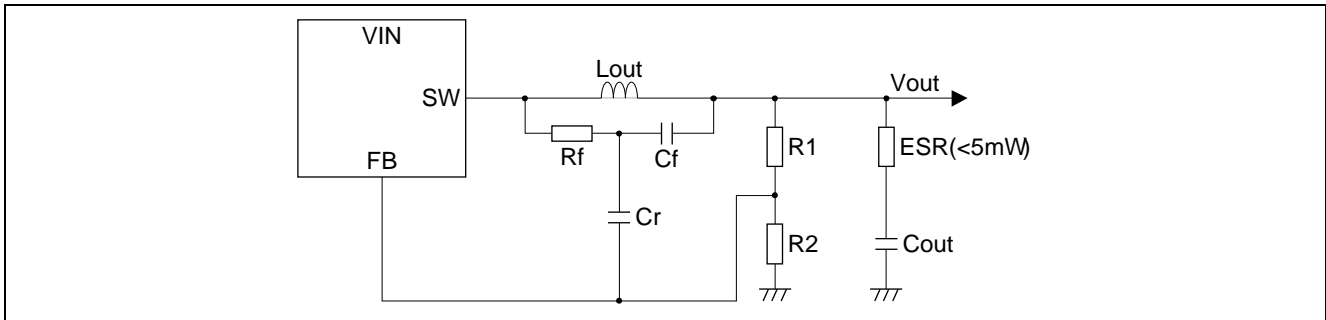
$$\text{Effective FB voltage (Vfb): } 0.8 \text{ V} + \frac{1}{2} ((\text{VIN} - \text{Vout}) \cdot \text{ton} \cdot \text{ESR} \cdot \text{R2} / (\text{Lout} \cdot (\text{R1} + \text{R2}))) \text{ [V] } \frac{1}{4} \text{ (7)}$$

Here, R1 and R2 is output voltage divider resistor, Lout is inductance of output filter and ESR means ESR of output capacitor (refer to above figure). 0.8 V in above equation means reference voltage of IC. Considering Vout ripple voltage, Vout voltage becomes below equation.

$$\text{Vout: } \text{Vfb} \cdot (\text{R1} + \text{R2}) / \text{R2 [V] } \frac{1}{4} \text{ (8)}$$

Operating with Small ESR Output Capacitor

When using low-ESR output capacitor like MLCC, voltage ripple on output voltage node is very small. So voltage ripple needs to be enhanced by additional components. Recommended ripple enhance method is like below figure.



Ripple injection on FB pin

\$R_f\$ and \$C_f\$ make ripple voltage using inductor DCR ripple. \$C_r\$ is used for AC ripple injection to FB pin. Ripple voltage between \$R_f\$ and \$C_f\$ is described by following equation.

$$V_{ripple}: (V_{IN} - V_{out}) \cdot t_{on} / (R_f \cdot C_f) [V] \quad (9)$$

$$R_f: (V_{IN} - V_{out}) \cdot t_{on} / (V_{ripple} \cdot C_f) [V] \quad (10)$$

Recommended ripple voltage is between 15 mV and 20 mV.

Stability criteria

To keep voltage ripple amplitude on FB pin, below equation should be satisfied.

$$\text{Stability criteria(1): } 1 / (2p \cdot C_f \cdot F_{sw}) \ll 1 / (2p \cdot C_r \cdot F_{sw}) \ll R_1 \cdot R_2 / (R_1 + R_2) \quad (11)$$

Here, \$F_{sw}\$ means switching frequency at CCM mode. Recommended value for \$C_f = 0.01 \text{ nF}\$, and \$C_r = 1000 \text{ pF}\$. \$R_1\$ and \$R_2\$ are recommended between 10 kW and 100 kW.

From loop stability analysis of above circuit configuration, the system must satisfy below equation.

$$\text{Stability criteria(2): } L_{out} \cdot C_{out} / (R_f \cdot C_f) > t_{on} / 2 \quad (12)$$

If the system cannot satisfy above equation, subharmonic oscillation will occur. Capacitance - voltage dependence is must be considered when MLCC use.

Vout setting

Additional ripple voltage and ESR voltage ripple also affects \$V_{out}\$ accuracy. From above figure, total ripple voltage on FB pin is described by below equation.

$$\text{Ripple voltage on FB pin: } (V_{IN} - V_{out}) \cdot t_{on} / (R_f \cdot C_f) + (V_{IN} - V_{out}) \cdot t_{on} \cdot \text{ESR} / (L_{out}) [V] \quad (13)$$

Effective FB pin voltage is described by below equation.

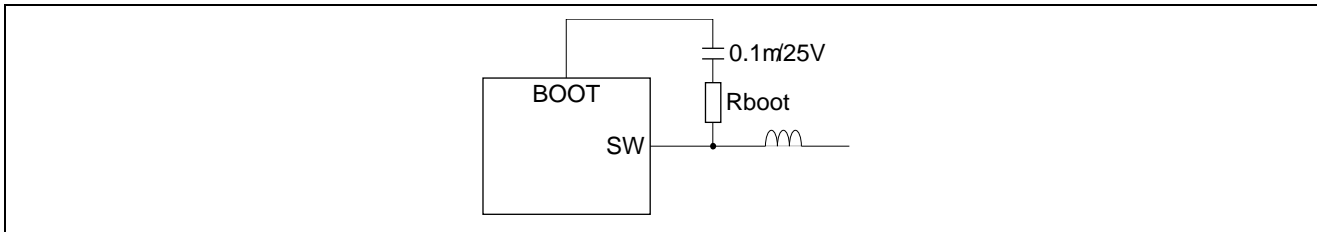
Effective FB voltage (\$V_{fb}\$):

$$0.8 V + \frac{1}{2} ((V_{IN} - V_{out}) \cdot t_{on} / (R_f \cdot C_f) + (V_{IN} - V_{out}) \cdot t_{on} \cdot \text{ESR} / (L_{out})) [V] \quad (14)$$

So, actual \$V_{out}\$ voltage is described by below equation.

$$V_{out}: V_{fb} \cdot (R_1 + R_2) / R_2 [V] \quad (15)$$

BOOT Resistance

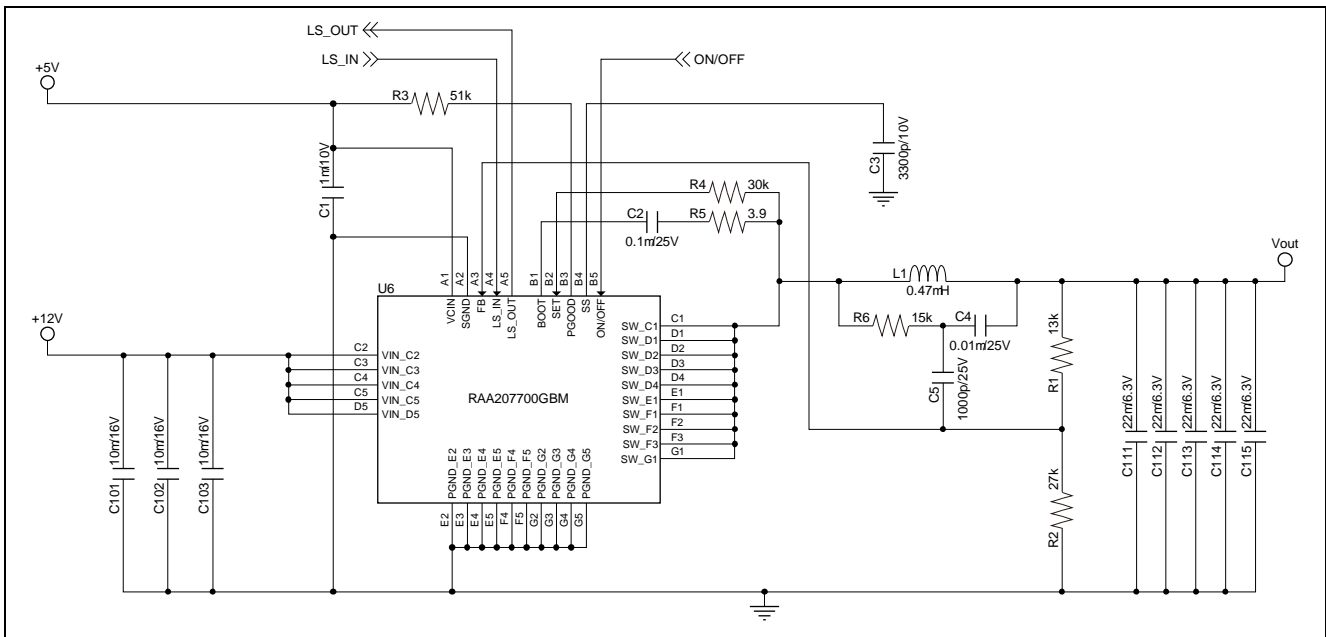


SW node spike occurs when IC is operating. Turn-on spike voltage exceeds absolute maximum voltage of SW pin depends on operating condition. To suppress the spike voltage, adding boot resistor (Rboot) is effective. Recommended Rboot is below.

Part No.	Recommended Rboot	
	VIN = 12 V	VIN = 5 V
RAA207700GBM	3.9 W	0 W
RAA207701GBM	2.0 W	0 W
RAA207702GBM	0 W	0 W

Design Example

(VIN = 12 V, VCIN = 5 V, Vout = 1.2 V, Fsw = 500 kHz (at CCM), L = 0.47 mH)



1. Setting of ton (constant on time)

In this condition, calculated on time is from equation (1),

$$\text{Calculated } t_{on}: 1.2 \text{ V} / 12 \text{ V} \cdot (1 / 500 \text{ kHz}) = 200 \text{ ns}$$

From equation (3),

$$\text{Calculated } R4 = (1.2 \text{ V} / (12 \text{ V} \cdot 500 \text{ kHz}) - 60 \text{ ns}) \cdot (12 \text{ V} - 2 \text{ V}) / (50 \text{ pF} \cdot 1 \text{ V}) = 28 \text{ kW}$$

so choose R4 = 30 kW from E24 series.

So, actual on pulse ton is decided by equation (2),

$$\text{Constant on time: } ((50 \text{ pF} \cdot 1 \text{ V} / (12 \text{ V} - 2 \text{ V})) \cdot 30 \text{ kW} + 60 \text{ ns}) = 210 \text{ ns}$$

2. Setting of ripple injection resistance

Voltage ripple on FB pin needs to be more than 15 mV. Here, C4 = 0.01 nF, C5 = 1000 pF and ESR of output cap = 0.5 mW. To obtain 15 mV additional ripple on FB pin from R6, C4 and C5 network circuit, R6 is calculated by equation (10).

$$\text{Calculated } R6: (12 \text{ V} - 1.2 \text{ V}) \cdot 210 \text{ ns} / (15 \text{ mV} \cdot 0.01 \text{ nF}) = 15.1 \text{ kW}$$

So choose R6 = 15 kW from E24 series and actual ripple voltage from injection circuit becomes 15.1 mV.

So, Total ripple voltage on FB pin is calculate by equation (13),

Total ripple voltage:

$$(12 \text{ V} - 1.2 \text{ V}) \cdot 210 \text{ ns} / (15 \text{ kW} \cdot 0.01 \text{ nF}) + (12 \text{ V} - 1.2 \text{ V}) \cdot 210 \text{ ns} / 0.47 \text{ mH} \cdot 0.5 \text{ mW} = 17.5 \text{ mV}$$

3. Setting of output voltage resistor

From above setting, effective FB voltage is from equation (15),

$$\text{Effective FB voltage: } 800 \text{ mV} + 17.5 \text{ mV} / 2 = 808.8 \text{ mV}$$

When R1 = 13 kW, R2 is decided from equation (15).

$$R2 = 13 \text{ kW} / ((1.2 \text{ V} / 808.8 \text{ mV}) - 1) = 26.8 \text{ kW}$$

So, choose R2 = 27 kW from E24 series.

4. Stability criteria confirmation

For output capacitor, please confirm stability criteria. Stability criteria from equation (11),

$$1 / (2p \cdot 0.01 \text{ nF} \cdot 500 \text{ kHz}) = 32 \text{ W} \ll 1 / (2p \cdot 1000 \text{ pF} \cdot 500 \text{ kHz}) = 318 \text{ W} \ll 13 \text{ kW} \cdot 27 \text{ kW} / (13 \text{ kW} + 27 \text{ kW}) = 8.8 \text{ kW}$$

so, above criteria is satisfied.

For output capacitor, please confirm stability criteria. Stability criteria from equation (12),

$$C_{out} > (210 \text{ ns} / 2) \cdot 15 \text{ kW} \cdot 0.01 \text{ nF} / 0.47 \text{ mH} = 34 \text{ nF}$$

So, choose 110 nF (22 nF ´ 5 pcs.) for output capacitor. Here, please consider voltage dependence of capacitor.

If you cannot satisfy above criteria, please consider below changes.

¾ increase L or Cout value

¾ increase frequency (decrease constant on time)

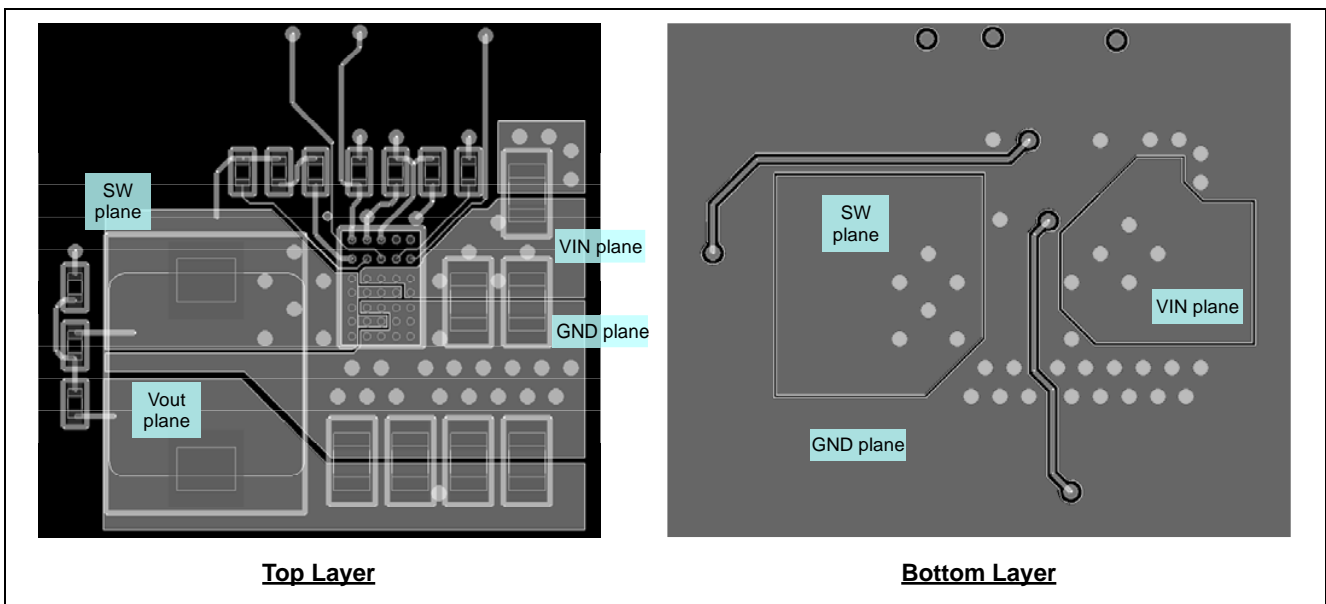
¾ change Rf value.

5. Other components

C1 = 1 nF / 10 V and C2 = 0.1 nF / 25 V are recommended. C3 decides soft start period from equation (5). R5 is decided from the table in "Boot Resistance" section. Input and output capacitors are decided considering voltage ripple, current ripple and voltage tolerance.

Board Layout Example (RAA207700GBM)

Board layer example: 4 layer, internal 2nd and 3rd layer are used for GND plane.



1. Power part
 - ¾ Input capacitor should be placed close to VIN and PGND pin to reduce switching noise and to improve the efficiency.
 - ¾ Many thermal via should be placed on VIN, SW and PGND planes to spread heat to board. Furthermore, VIN, SW planes on bottom layer are effective for thermal spread (If available).
2. Control part
 - ¾ Decoupling capacitor between VCIN and SGND should be placed as close as possible to the chip in order to stable operation.
 - ¾ Also, SGND, PGND via should be placed as close as possible to the chip, and connect each pin low impedance by internal GND plane.
 - ¾ FB resistance should be placed close to chip and FB wiring should be short to avoid noise. Furthermore, additional ripple circuit wiring should be kept away from high dv/dt plane such as SW and BOOT wiring.
 - ¾ To ensure the reliability of chip - board connection, we recommend Solder Mask Defined (SMD) layout. But you can also use Non-Solder Mask Defined (NSMD) layout as far as you can ensure the reliability. In the case of SMD layout, we recommend below size.
Solder resist open size: 280 μm , Land size: 280 μm + 50 to 100 μm (please consider processing accuracy)
3. Line SW
 - ¾ When Line SW function is not used, no need to wiring LS_IN, LS_OUT pin.

Representative Inductors

Maker	Inductance [nH]	DL/L0 = 20% Change [A]	Dimensions [mm]
NEC Tokin MPC series	0.42	20.0	6.7 ´ 8.0 ´ 4.0
	0.60	19.0	6.7 ´ 8.0 ´ 5.0
	0.88	24.0	10.0 ´ 11.5 ´ 4.0
	1.0	25.0	10.0 ´ 11.7 ´ 5.5
ALPS Green Device GLMC series	0.47	13.9 *1	6.5 ´ 7.4 ´ 3.0
	1.0	10 *1	6.5 ´ 7.4 ´ 3.0
	1.5	8.8 *1	6.5 ´ 7.4 ´ 3.0
TOKO FDVE0630 series	0.33	15.9	6.7 ´ 7.4 ´ 3.0
	0.47	15.6	6.7 ´ 7.4 ´ 3.0
	0.75	10.9	6.7 ´ 7.4 ´ 3.0
	1.0	9.5	6.7 ´ 7.4 ´ 3.0
TDK SPM5030 series	0.35	14.9	5.0 ´ 5.2 ´ 3.0
	0.47	11.0	5.0 ´ 5.2 ´ 3.0
	0.75	9.7	5.0 ´ 5.2 ´ 3.0

Note: *1 30% change

- Small size inductor for RAA207702GBM

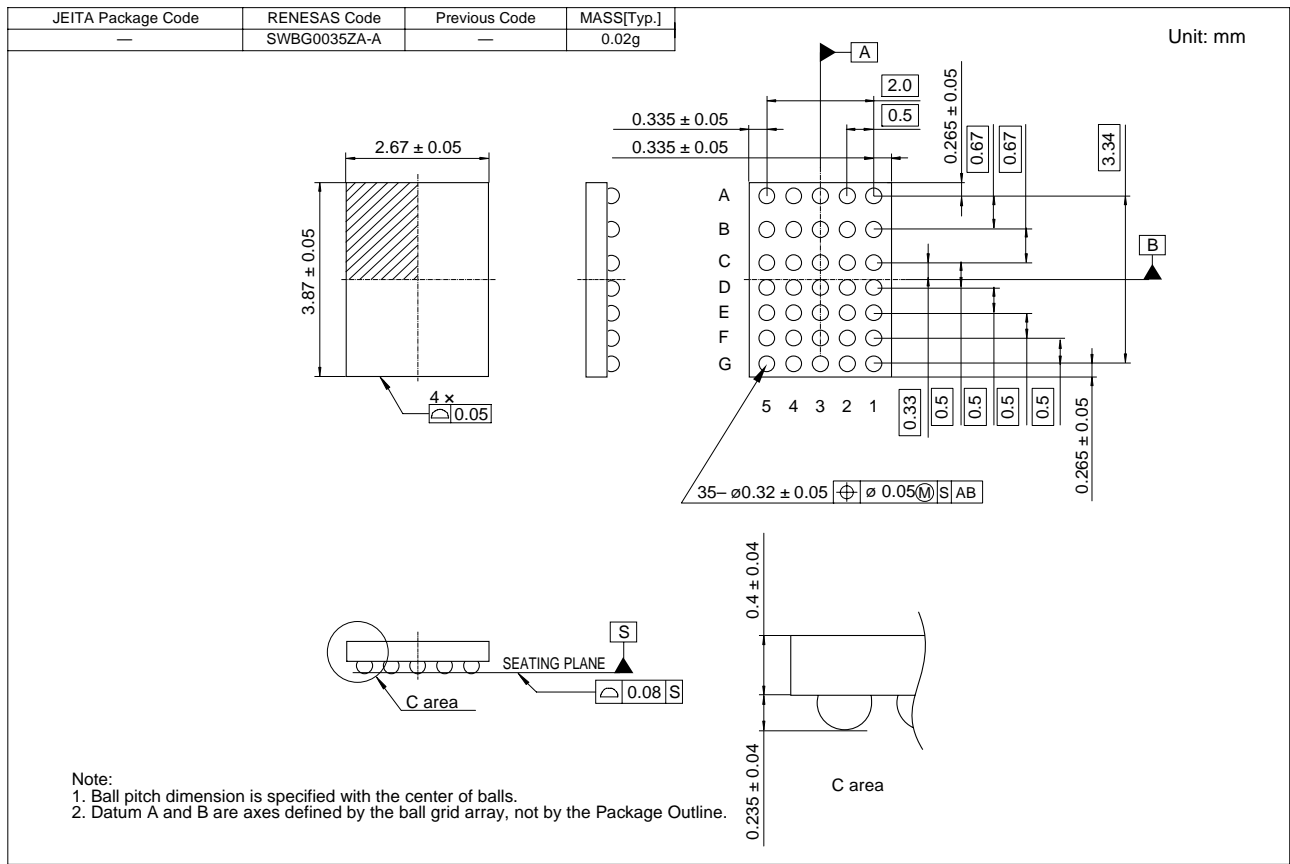
Maker	Inductance [nH]	DL/L0 = 30% Change [A]	Dimensions [mm]
TOKO FDSD0420 series	0.68	8.3	4.2 ´ 4.2 ´ 2.0
	1.0	6.8	4.2 ´ 4.2 ´ 2.0
	1.5	5.7	4.2 ´ 4.2 ´ 2.0
TDK SPM4012 series	0.47	8.3	4.4 ´ 4.1 ´ 1.2
	1.0	4.8	4.4 ´ 4.1 ´ 1.2

Representative Output Capacitors

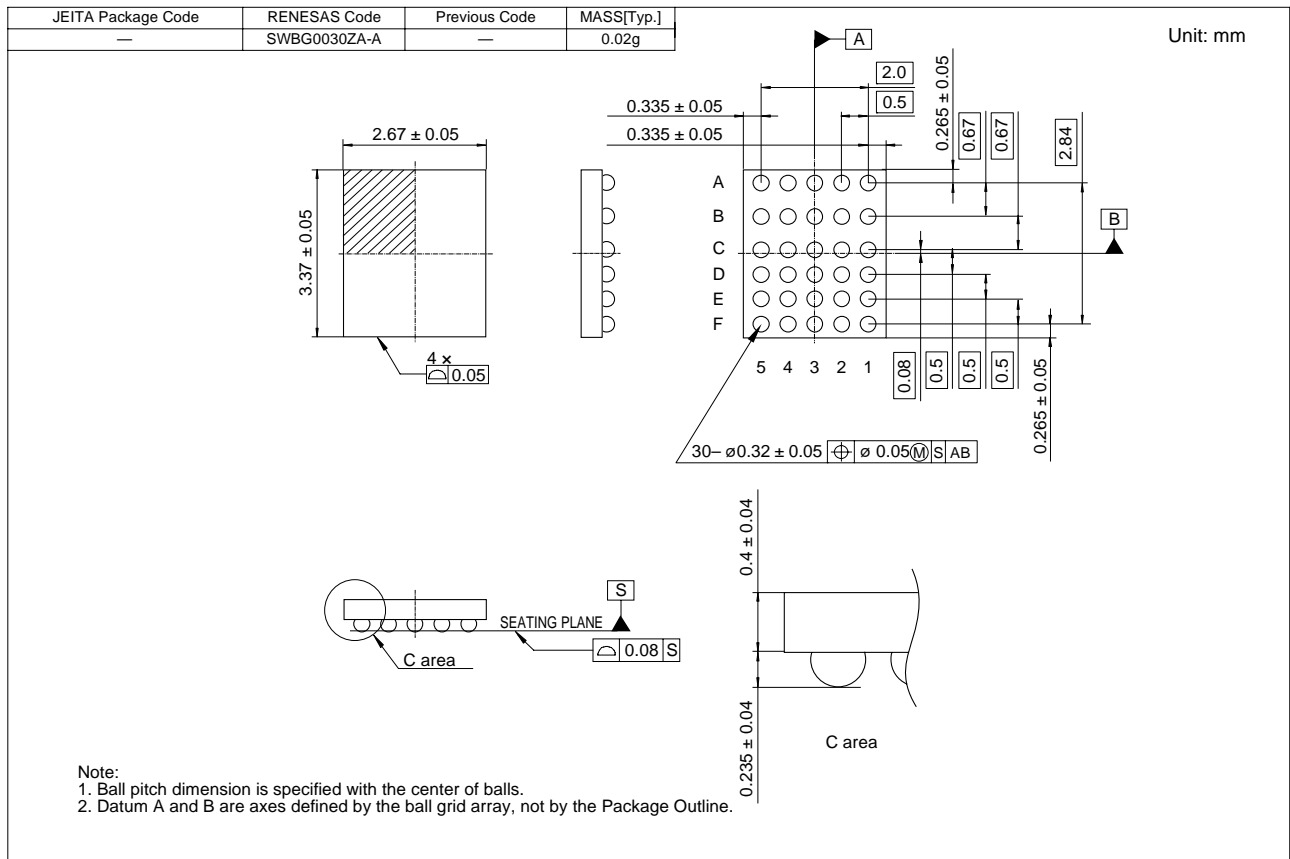
Maker	Maximum Voltage [V]	Capacitance [nF]
Sanyo POSCAP series	2.0 to 10	47 to 330
Sanyo OS-CON series	2.0 to 10	47 to 330
Murata MLCC series	6.3 to 10	22 to 47
TDK MLCC series	6.3 to 10	22 to 47
TAIYO YUDEN MLCC series	6.3 to 10	22 to 47

Package Dimensions

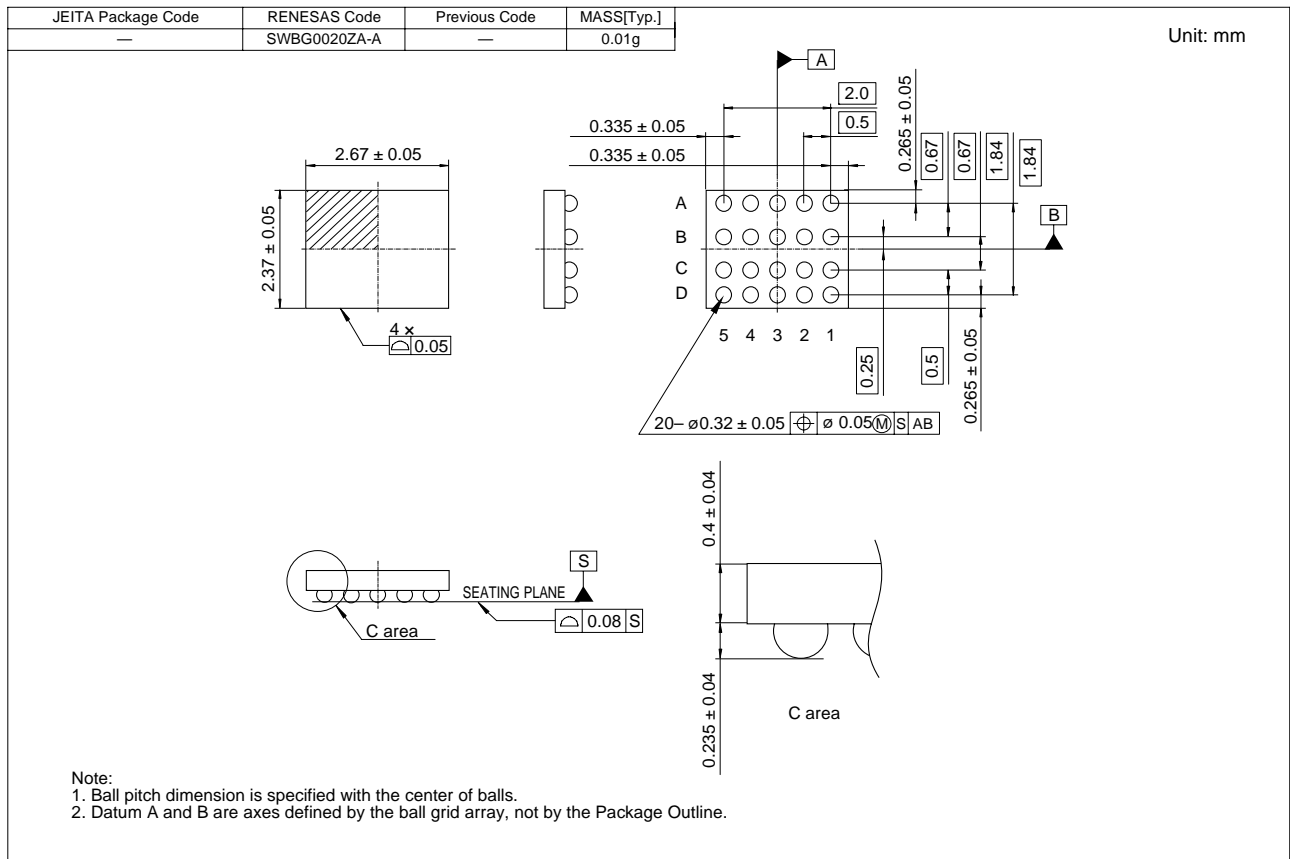
• RAA207700GBM



· RAA207701GBM



RAA207702GBM



Ordering Information

Part Name	Quantity	Shipping Container
RAA207700GBM#HC0	2000 pcs	Taping Reel
RAA207701GBM#HC0	2000 pcs	Taping Reel
RAA207702GBM#HC0	2000 pcs	Taping Reel

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