# UG0173
# User Guide
# Fusion Advanced Development Kit

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# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 2.1

The following is a summary of the changes in revision 2.1 of this document.

- Changed Actel to Microsemi throughout the document.
- Libero SoC software license information was updated from Gold to Silver. For more information, see Software Installation, page 6.

## 1.2 Revision 2.0

There were no changes to the technical content in revision 2.0 of this document.

## 1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

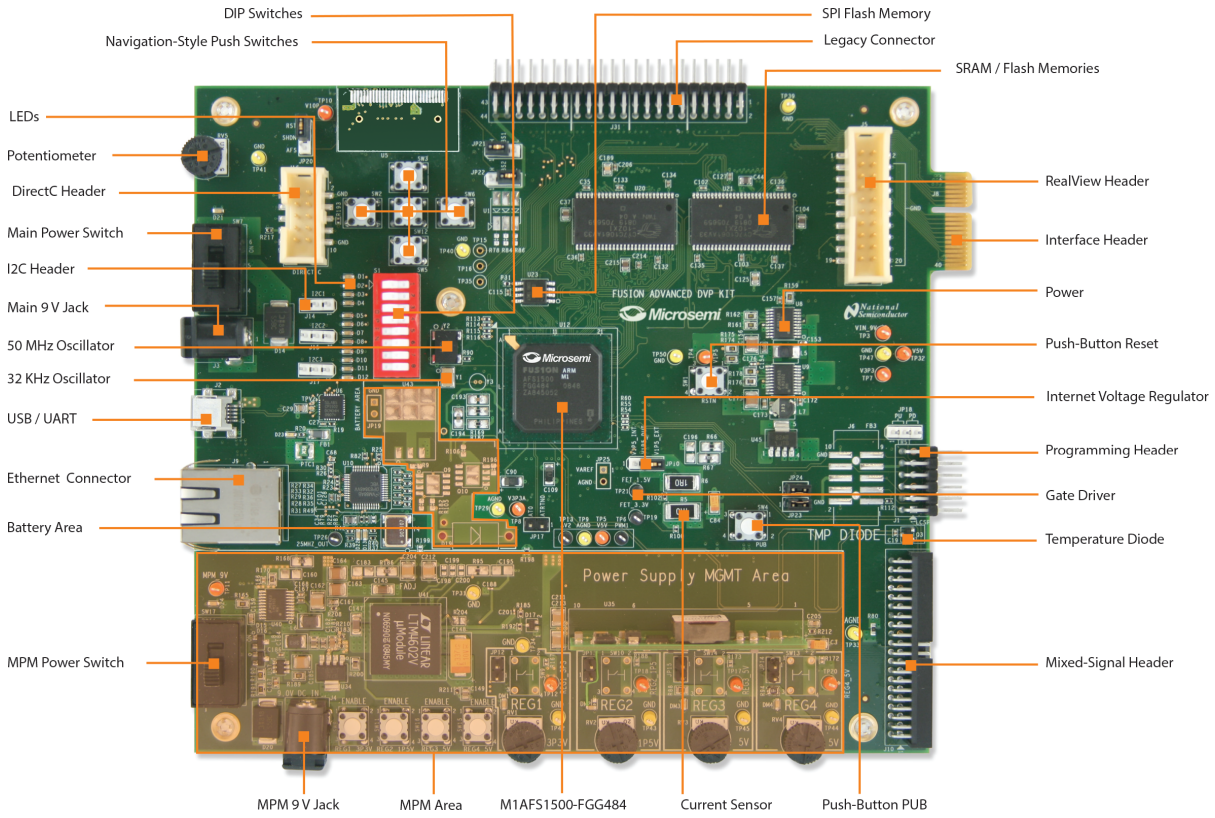
# 2 Introduction

The RoHS-compliant Fusion Advanced Development Kit helps designers in developing applications that involve one or more of the following:

- Power sequencing
- System management
- Embedded ARM Cortex-M1–based systems

The board also provides a standard 40-pin mixed-signal header for interfacing to the analog pins. This provides access for plugging in a daughter board with mixed-signal interface.

***Figure 1 •*** **Fusion Advanced Development Kit**




## 2.1 Kit Contents–M1AFS-ADV-DEV-KIT-PWR-2

The following table lists the contents of the Fusion Advanced Development Kit.

***Table 1 •*** **Fusion Embedded Development Kit Contents**

| Item | Quantity |
|---|---|
| Fusion Advanced Development Kit board with ARM Cortex-M1–enabled M1AFS1500-FGG484 | 1 |
| FlashPro3-compatible low-cost programming stick (LCPS) | 1 |
| Mini universal serial bus (USB) cables | 2 |
| Quickstart card | 1 |

**Note:** M1FAS-ADV-DEV-KIT does not include power supplies, so for this kit you must also order two of the 9V POWER PACKs. M1AFS-ADV-DEV-KIT-PWR-2 includes the one 9 V power pack.

## 2.2 Fusion Advanced Development Kit Web Resources

For further kit information, including user's guides, tutorials, and full design examples, refer to the Fusion Advanced Development Kit page:
www://soc.microsemi.com/products/hardware/devkits_boards/fusion_adv.aspx.

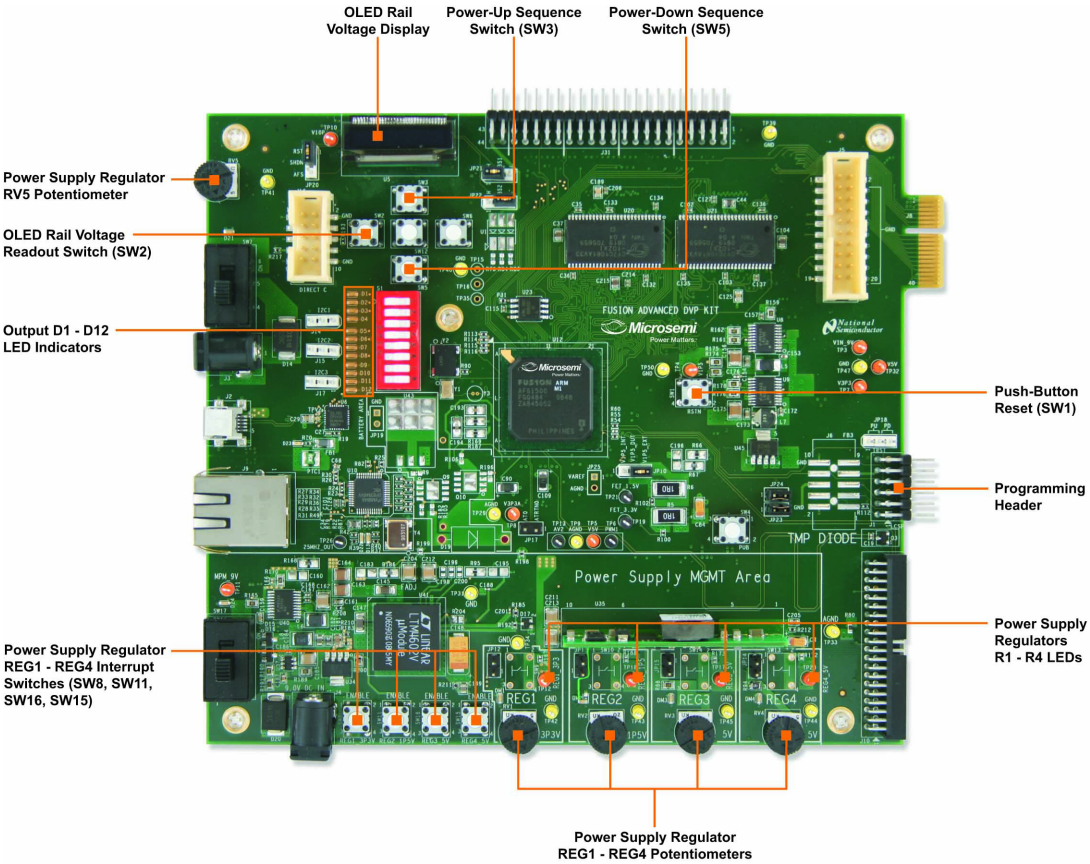
Resources include:

- Microsemi Libero® Integrated Design Environment (IDE) v8.5 User Guide
- FlashPro v8.5 User's Guide
- Mixed-Signal Power Manager User Guide
- ARM Cortex-M1 Embedded Processor Hardware Development Tutorial
- ARM Cortex-M1 Embedded Processor Software Development Tutorial
- Core8051s Embedded Processor Hardware Development Tutorial
- Core8051s Embedded Processor Software Development Tutorial

## 2.3 Mixed-Signal Power Manager Demonstration

The Mixed-Signal Power Manager demonstrator is a reference design targeted to the Fusion Advanced Development Kit that delivers superior power monitoring, power sequencing, and threshold control of up to 16 power regulators. Users can configure power management sequencing, levels, or thresholds using an easy-to-use standalone graphical user interface (GUI) tool, which also enables the user to program the MPM design into the Fusion device. Designers using MPM will be able to replace discrete power management devices, add more flexibility by leveraging Fusion's reprogrammable flash FPGA technology, and reduce total parts count at the board level. MPM will deliver highly-configurable, integrated power management using one high-reliability low-power flash-based Fusion mixed-signal FPGA. The MPM user's guide and zip file are available from the Fusion Advanced Development Kit page.

***Figure 2 •*** **Fusion Advanced Development Kit Board for Mixed-Signal Power Manager**




## 2.4 Board Description

The Fusion Advanced Development Kit board provides a low-cost board for the system management platform, using the Fusion FPGA's advanced features, such as mixed-signal analog and embedded processor.

The board also provides a mixed-signal power management (MPM) circuitry that can be used for sequencing and management. You can use the MPM for power management as it is done in application-specific standard products (ASSPs). The MPM tool enables you to configure each of the available voltage channels, without the need to explore details of the FPGA part on the board.

The evaluation board supports a Cortex-M1 embedded processor on a Fusion device in the FGG484 package. To enable embedded system management the evaluation board includes the following:

- Ethernet and USB-to-UART interface for communication with the Fusion FPGA
- SRAM, parallel flash, and SPI flash
- Temperature diode, potentiometer, and pulse-width modulation (PWM) circuit
- Mixed-signal header for several daughter boards to be attached for extended mixed-signal applications

The board includes a programming stick header so the LCPS can be attached to the board for programming.

The following table lists the Fusion Advanced Development Kit board components.

***Table 2 •*** **Fusion Advanced Development Kit Board Components**

| Name | Description |
|---|---|
| M1AFS1500-FGG484 | Microsemi Fusion mixed-signal FPGA |
| PWM CIRCUIT | PWM circuit |
| POT CIRCUIT | Potentiometer connected to the analog pin of the Fusion device |
| CURRENT SENSING | Two circuits for 1.5 V and 3.3 V current monitoring |
| TEMP MONITOR DIODE | External temperature diode connected to the Fusion device |
| GATE DRIVER | Two external p-channel MOSFET |
| OSC-50 | 50 MHz clock oscillator |
| OSC-32 | 32.768 KHz off-chip crystal oscillator |
| PUSH-BUTTON RESET | System reset with Schmitt trigger |
| LEDS | 12-RED (4 more in production boards) |
| DIPSWITCH | 8 signals |
| PUSHSWITCH | 7 signals |
| I2C HEADER | 3 ports for I2C interface |
| INTERFACE CONNECTOR | 38-pin finger header |
| RVI HEADER | RealView interface header for M1 debugging |
| ETHERNET | 10/100 interface |
| USB/UART | USB/UART adapter chip and connector |
| BATTERY (not populated) | On-board battery slot for charging |
| SRAM | 4 MB (2 × 1M × 16) Cypress CY7C1061DV33-10ZSXI |
| FLASH | 64 Mbit parallel flash memory (2 × 1M × 16) Numonyx JS28F640J3D-75 |
| SPI FLASH | SPI-based flash device 2 MB Atmel AT45DB161D-SU |
| PROG HDR | DirectC programming header |
| MIXED_CONN40 | Mixed-signal header |
| LC_JTAG | Low-cost programming stick |

The following table lists the Mixed-Signal Power Manager board components.

***Table 3 •*** **Mixed-Signal Power Manager Board Components**

| Component | Description |
|---|---|
| MPM_REG1_3P3 | 3.3 V regulated supply, National LM3100MH |
| MPM_REG2_1P5 | 1.5 V regulated supply, National LP38693-ADJ |
| MPM_REG3_5V | 5 V regulated supply 1, Lineage Power ATA010A0X43 |
| MPM_REG4_5V | 5 V regulated supply 2, Linear Technology LTM 4602 |
| RV1, RV2, RV3, RV4 | POT to vary the voltage o/p of the regulator |
| SW8, SW11, SW15, SW16 | Switch to enable/disable MPM voltage regulators |

# 3 Installation and Settings

This section provides information about software and hardware settings required to run the pre-programmed demo design in the Fusion Advanced development Kit.

## 3.1 Software Installation

Download and install the latest release of Libero SoC from the Microsemi website and register for your free Silver license. For instructions on how to install Libero SoC and SoftConsole, see the *Libero Software Installation and Licensing Guide*

## 3.2 Hardware Installation

The FlashPro3 programmer is built into the low-cost programming stick (LCPS) and plugs directly into the FADK board. The USB 2.0 high-speed cable plugs into the LCPS to allow the M1AFS1500 device to be programmed.

## 3.3 Jumper and Switch Settings

Recommended default jumper settings are defined in the following table. Connect the jumpers with the default settings to enable the pre-programmed demonstration design to function correctly.

***Table 4 •*** **Fusion Advanced Development Kit Jumper Settings**

| Jumper | Function | Default Setting |
|---|---|---|
| JP10 | Jumper to select either 1.5 V external regulator or Fusion 1.5 V internal regulator.<br>Pin 1–2 = 1.5 V internal<br>Pin 3–2 = 1.5 V external | Pin 3–2 |
| JP17 | Analog temperature out (AT0) to analog temperature return (ATRNT0) | Header to external temperature monitor diode |
| JP18 | Jumper to select TRST High or Low.<br>Pin 1–2 = High (V3P3_AFS)<br>Pin 2–3 = Low (GND) | Pin 2–3 |
| JP20 | Power sequencing for 10 V rail<br>1–2: Use a reset chip to provide 100 ms delay on the 10 V rail<br>2–3: Use Fusion gate drivers to provide 100 ms delay on the 10 V rail | Pin 1–2 |
| JP21 | OLED_BS1<br>1–2: V3P3<br>2–3: GND | Pin 1–2[1] |
| JP22 | OLED_BS1<br>1–2: V3P3<br>2–3: GND | Pin 2–3[1] |
| JP23 | $V_{JTAG}$ to V3P3_AFS | Pin 1–2 |
| JP24 | $V_{PUMP}$ to V3P3_AFS | Pin 1–2 |

1. The latest revision of Fusion Advanced development kit (M1AFS-ADV-DEV-KIT-PWR-2) does not contain OLED display on the board.

The following table lists the mixed-signal power manager jumper settings.

***Table 5 •*** **Mixed-Signal Power Manager Jumper Settings**

| Jumper | Function | Default Setting |
|---|---|---|
| JP12 | Jumper from FB (feedback voltage) pin of 3.3 V regulator to Fusion for voltage trimming | Closed |
| JP13 | Jumper from ADJ (adjust voltage) pin of 1.5 V regulator to Fusion for voltage trimming | Closed |
| JP14 | Jumper from Voset (voltage) pin of 5 V DC-DC regulator to Fusion for voltage trimming | Closed |
| JP15 | Jumper from Trim (voltage) pin of 5 V DC-DC convertor output to Fusion for voltage trimming | Closed |

The following table lists the Fusion Advanced Development Kit push-button switches.

***Table 6 •*** **Fusion Advanced Development Kit Push-Button Switches**

| Push-Button Switch | Comment |
|---|---|
| SW1 | System reset for DUT |
| SW4 | Push-button switch for PUB. This negative active switch is connected to the PUB pin, which is a digital input to the Fusion FPGA. PUB is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator 3. |
| SW7 | Switch ON 9 V DC into Fusion supply regulators |
| SW2 | Test and navigation switch |
| SW3 | Test and navigation switch |
| SW5 | Test and navigation switch |
| SW6 | Test and navigation switch |
| SW12 | Test and navigation switch |

The following table lists the mixed-signal power manager push-button switches

***Table 7 •*** **Mixed-Signal Power Manager Push-Button Switches**

| Push-Button Switch | Comment |
|---|---|
| SW17 | Switch ON 9 V DC into MPM |
| SW8 | Push-button to disable 3.3 V supply regulator |
| SW11 | Push-button to disable 1.5 V supply regulator |
| SW16 | Push-button to disable 5 V supply regulator |
| SW15 | Push-button to disable 5 V supply regulator |

**CAUTION**: The push-buttons SW8, SW11, SW15, and SW16 ground the enable pin of the corresponding regulator, thereby injecting failure in the power subsystem. However, this enable pin is also connected to the pin on the Fusion FPGA (MPM_REG1_EN, MPM_REG2_EN, MPM_REG3_EN, MPM_REG4_EN). The FPGA would be damaged if it were driven High on the enable line and grounded at the same time. To avoid this, Microsemi recommends that the FPGA pin driving these enable pins is set to Low or tristate.

The following table lits the Fusion Advanced Development Kit test points.

***Table 8 •*** **Fusion Advanced Development Kit Test Points**

| Test Point | Comment |
|---|---|
| TP3 | 9 V input |
| TP4 | 1.5 V supply rail |
| TP7 | 3.3 V supply rail |
| TP8 | 3.3 V supply AFS |
| TP10 | 10 V rail for OLED |
| TP19 | 3.3 V voltage and current sensing circuit |
| TP21 | 1.5 V voltage and current sending circuit |
| TP39, TP40, TP41, TP47, TP50 | GND |
| TP29, T33 | Analog ground |
| TP32 | 5 V supply |
| TP5 | 5 V supply |
| TP6 | PWM1 |
| TP9 | AGND |
| TP13 | AV2 |

**Note:** Tests points TP13 (AV), TP9 (AGND), TP5 (V5V), and TP6 (PWM1) provide the capability of hooking up any external Power Regulator Evaluation Board with an input voltage of 5 V. The Fusion FPGA can be used for voltage monitoring and trimming on this board.

The following table lits the mixed-signal power manager test points

***Table 9 •*** **Mixed-Signal Power Manager Test Points**

| Test Point | Comment |
|---|---|
| TP11 | 9 V supply for MPM |
| TP12 | 3.3 V supply (regulated supply 1) |
| TP18 | 1.5 V supply (regulated supply 2) |
| TP17 | 5 V supply (regulated supply 3) |
| TP20 | 5 V supply (regulated supply 4) |
| TP31, TP34, TP42, TP 43, TP 44, TP45 | MPM GND |

## 3.4 Testing the Hardware

If the board is shipped directly from Microsemi, it contains a test program that determines whether the board works properly. If while using the board you suspect that the board is damaged, you can rerun the Manufacturing Test, page 38 to verify the key components of the board functionality.

# 4 Hardware Components

## 4.1 FPGA Description and Connections

The Fusion Advanced Development Kit board is populated with an M1-enabled Fusion M1AFS1500 FPGA. The key features of the M1AFS1500 device are listed below:

- High-performance reprogrammable flash technology
- Embedded flash memory
- Integrated A/D converter (ADC) and Analog Quad
- On-chip clocking resources
- Low power consumption
- In-system programming (ISP) and security
- Advanced digital I/Os
- SRAMs and FIFOs

The following table lists the key features of the M1AFS1500 device.

***Table 10 •*** **M1AFS1500 Key Features**

| Feature | Description |
|---|---|
| System Gates | 1,500,000 |
| Tiles (D-flip-flop) | 3,840 |
| Secure (AES) ISP | Yes |
| PLLs | 2 |
| Global Routing Resources | 18 |
| Total Flash Memory Bits | 8 M (2-Mbit blocks x 4) |
| FlashROM Bits | 1 k |
| RAM Blocks (4,608 bits) | 60 |
| RAM kbits | 270 |
| Analog Quads | 10 |
| Analog Input Channels | 30 |
| Gate Driver Outputs | 10 |
| I/O Banks (+JTAG) | 5 |
| Maximum Digital I/Os | 252 |
| Analog I/Os | 40 |

For more information about Fusion, see the *Fusion Mixed-Signal FPGAs Datasheet* and *Fusion and Extended Temperature Fusion FPGA Fabric User*.

### 4.1.1 I/O Pins Connection on M1AFS1500-FGG484

The M1AFS1500-FGG484 pin list is provided in the Pin List, page 30.

### 4.1.2 Fusion FPGA Advanced Microprocessor

Microsemi offers several microprocessor and microcontroller solutions for developers, all of which are tightly integrated with Microsemi Libero SoC, optimized for Microsemi FPGA architecture, and supplied with a complete toolset for code compile and debug.

The Fusion Advanced Development Kit board contains a Fusion M1AFS1500 FPGA device, which is Cortex-M1– enabled. Cortex-M1 is the first ARM processor developed specifically for implementation in FPGAs. In addition to Cortex M1, this Fusion FPGA can be programmed with Core8051(s) or CoreABC.

A few components are populated on the Embedded Development Kit board for basic Cortex-M1 development. These components include SRAM, SPI-based flash, ethernet interface, USB-to-UART bridge, EEPROM, and I2C interfaces. To integrate these components into a complete solution, Microsemi supplies a full range of subsystem IP cores: memory controllers, timers, mailbox, serial interface controllers, and others. These subsystem IP can connect to the embedded processor via the advanced microcontroller bus architecture (AMBA) bus.

Refer to Microsemi's IP catalog for additional information on available IPs for Fusion M1-enabled embedded processors: https://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

## 4.2 Power Sources

There are two separate external 9 V power supply bricks: one for the Fusion FPGA part of the board and other for the MPM part of the circuitry. If you are not using MPM, you will need only one 9 V power supply brick.

### 4.2.1 Fusion FPGA Power Sources

Three voltage rails (10 V, 3.3 V, and 1.5 V) are provided on the board through the 24 V tolerant regulators:

- A single regulator, National 3102MH (3.3 V, 1.25 A), supplies both analog and digital 3.3 V going to the Fusion device. Sufficient isolation is provided through low-pass filter and layout to prevent noise from the digital domain interfering on the analog domain.
- National LM3100 MH (1.5 V, 500 mA) supplies the 1.5 V rails.
- National LM27313 boost converter supplies 10 V, 100 mA typical, for driving OLEDs.

**Note:** The 10 V supply for the OLED must have power sequencing for maintaining a 100 ms delay between 3.3 V and 10 V, where 3.3 V powers up first. This can be achieved through jumper JP20 by using a National reset circuitry (LM 3722), or using M1AFS gate drivers to do the power-up sequencing.

**Note:** This board is not designed to power up external daughter boards. Microsemi recommends to run a detailed power analysis when designing for daughter boards which require to be powered up form the main board.

**Note:** The latest revision of Fusion Advanced development kit (M1AFS-ADV-DEV-KIT-PWR-2) does not contain OLED display on the board.

### 4.2.2 MPM Power Sources

This part of the circuit uses 4 voltage supply regulators:

- LDO regulator 1.5 V
- Switching regulator 3.3 V
- DC-DC regulators 5 V
- DC-DC regulators 5 V

All the regulators are supplied by one external 9 V brick.

**Note:** The Fusion Advanced Development Kit needs two external power supplies (9 V) for board operation; one for the Fusion device and one for the regulators in the MPM circuitry. Since MPM is using the Fusion device to monitor the multiple power rails coming out of regulators, you cannot use the same 9 V power supply to power-up the Fusion design and supply power to the input of the regulators that it is monitoring.

## 4.3 Mixed-Signal Power Management

This part of the circuitry consists of four sets of regulated power supplies running from a 9 V supply:

- National LDO regulator, 1.5 V
- National switching regulator, 3.3 V
- Linear DC-DC regulator, 5 V
- Artesyn DC-DC regulator, 5 V

The MPM tool can be used for these tasks:

- Monitoring voltage for all rails
- Sequencing different power rails for power-up and power-down
- Trimming and margining voltage rails in a closed loop
- Sweeping the output voltage (POT circuit to change resistor on feedback voltage)
- Inducing failures by disabling the enable input of the regulator (push-button to GND enable)

Power sequencing is done by sequentially asserting or deasserting channel enable pins for power-up and power-down, respectively, and monitoring the associated channel voltage. All Enable pins to the regulator are active High.

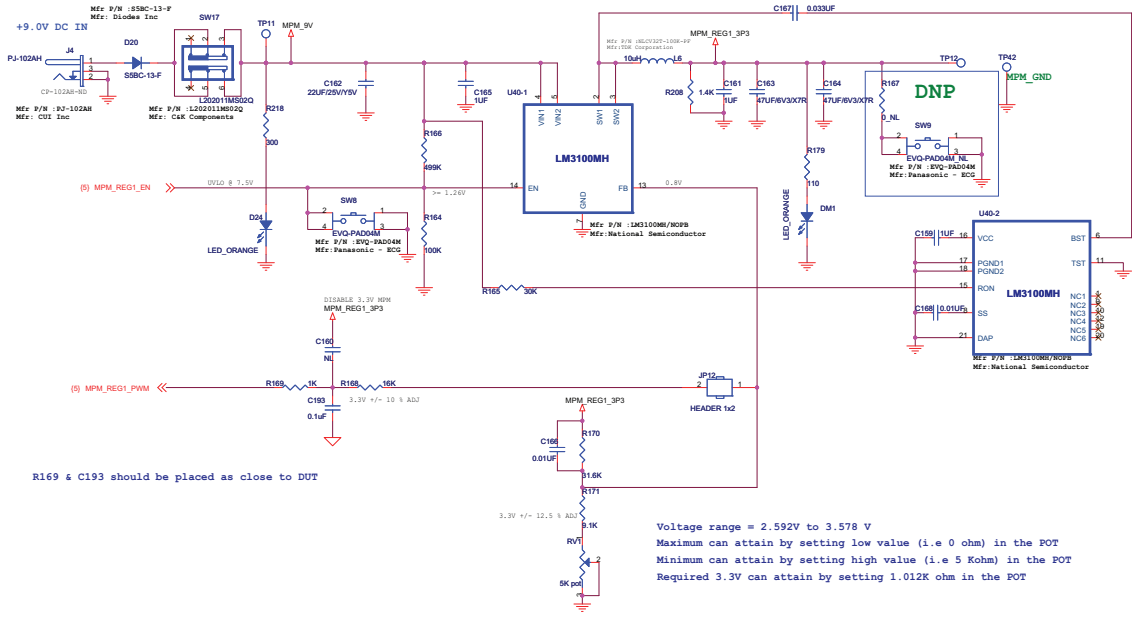
**Note:** For more information about the MPM circuit functionality and a design example for the MPM GUI, see *SmartFusion2 DMPM Kit QuickStart Guide*.

# 4.4 Board Components for Power Management

## 4.4.1 3.3 V Power Supply, MPM_REG1_3P3, National LM3100MH

This regulated switching mode power supply can deliver up to 1.5 A of output current with regulated output voltage from 0.8 to 5.0 VDC, over a wide range of input voltage ($V_{IN}$ = 4.5–36 VDC). Different output voltages can be set by changing the value of feedback voltage on the feedback pin (FB) using a resistor feedback divider.

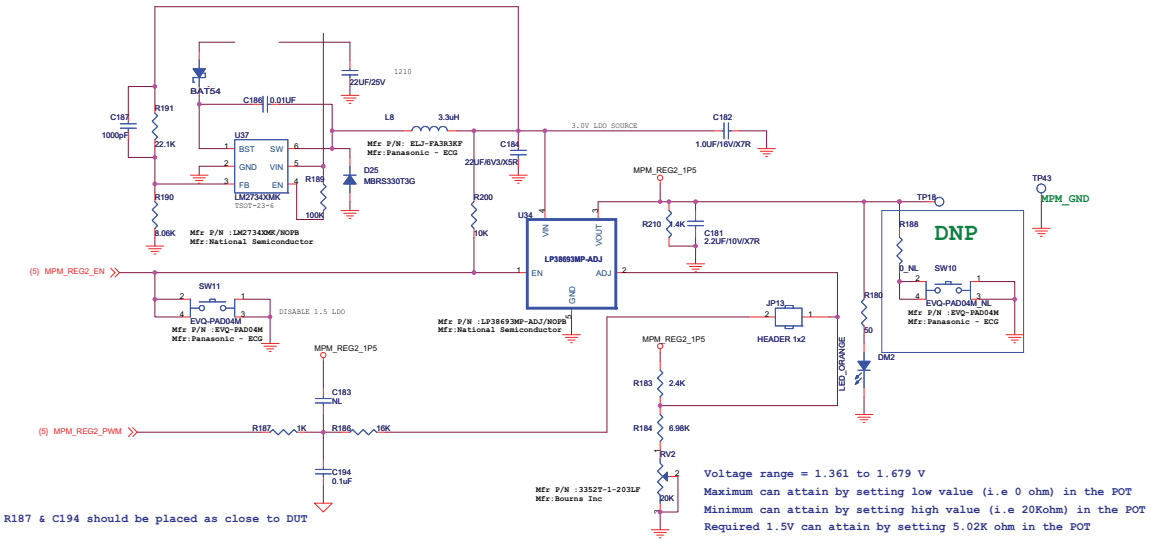
***Figure 3 •*** **MPM Switching Power Supply, 3.3 V**



## 4.4.2 1.5 V Power Supply, MPM_REG2_1P5, National LP38693-ADJ

This is a low drop-out voltage regulator (250 mV at 500 mA with 5 V o/p) with output voltage ranging from 1.25 V to 9 V. The input has a wide range from 2.7 V to 10 V. The output voltage can be set by controlling the voltage feedback input to ADJ. Pulling the enable pin down to a logic low will turn the part off.

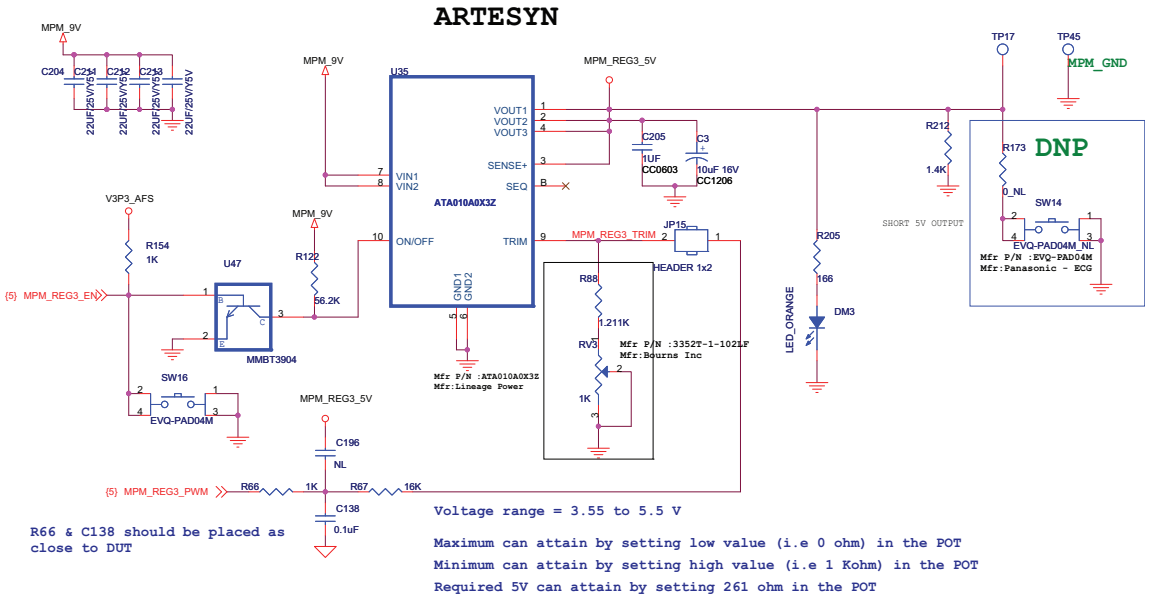
***Figure 4 •*** **MPM Low Drop-Out Power Supply, 1.5 V**




## 4.4.3 5 V Power Supply 1, MPM_REG3_5V, Lineage Power ATA010A0X43

The 12 V single in-line package (SIP) power module can deliver up to 10 A of output current with regulated output voltage from 0.75 to 5.0 VDC, over a wide range of input voltage ($V_{IN}$ = 8.3–14 VDC). The output voltage can be controlled using an external resistor between the TRIM and the GROUND pins of the module.

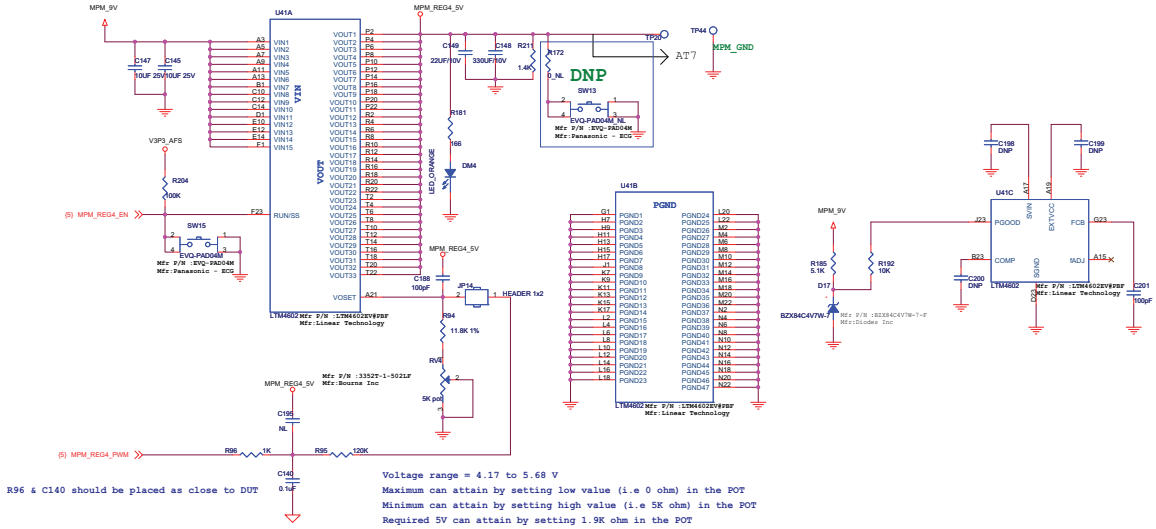
***Figure 5 •*** **MPM DC-DC Power Supply, 5 V**



## 4.4.4 5 V Power Supply 2, MPM_REG4_5V, Linear Technology LTM 4602

This DC/DC converter can deliver up to 6 A of output current with regulated output voltage from 0.6 to 5.0 VDC, over a wide range of input voltage ($V_{IN}$ = 4.5–20 VDC). Different output voltages can be programmed using resistors between the VOSET and SGND pins.

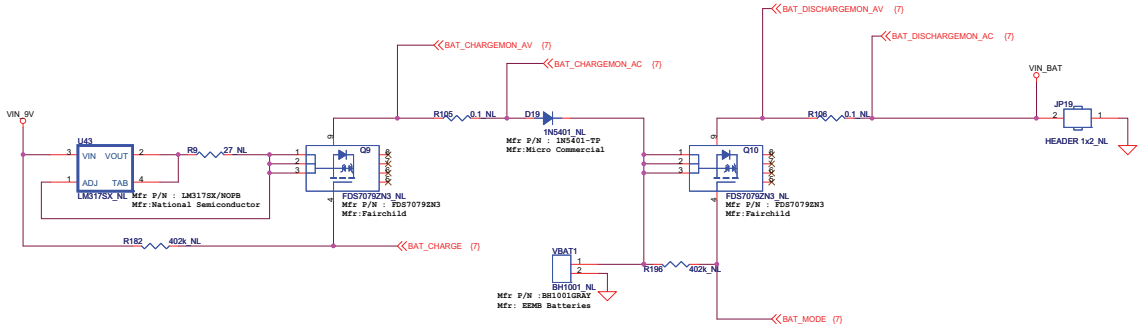
***Figure 6 •*** **MPM DC-DC Power Supply 2, 5 V**




## 4.4.5 Battery Charging

The battery-charging application within the MPM infrastructure demonstrates the charging/discharging of a Lion LIR2450 rechargeable battery. Gate drivers in combination with field-effect transistors (FETs) can be used to charge or discharge the battery. The output of this battery is made available to headers, with the ability to plug-in an Icicle Board and provide five to six hours of battery life.

***Figure 7 •*** **Battery Charging and Discharging Circuit**

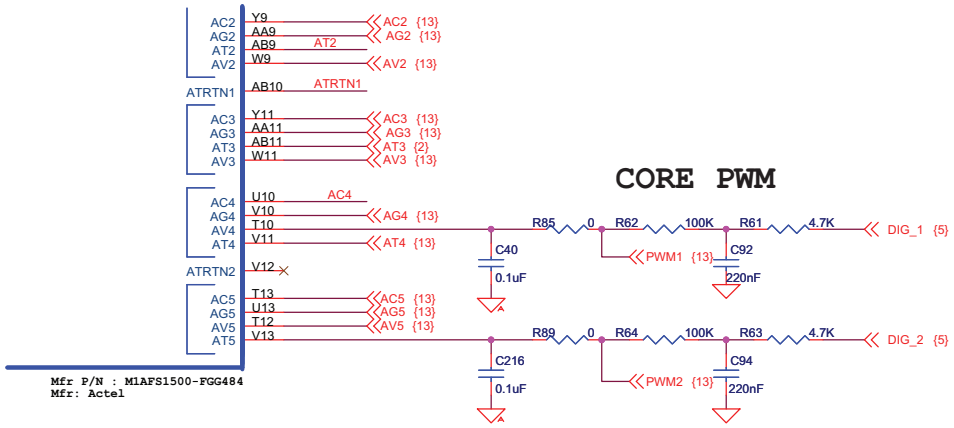



# 4.5 Components Descriptions and Connections

## 4.5.1 PWM Circuit

The PWM RC circuit can be used with CorePWM instantiated in the FPGA fabric to generate various voltages waveforms. These voltage waveforms can be displayed on the OLED or used via the mixed-signal header. In addition, one PWM RC circuit source is routed to the AV input pin of an analog quad. This AV pin can be used to monitor the generated voltage with high accuracy, depending on the ADC resolution configured in the FPGA.

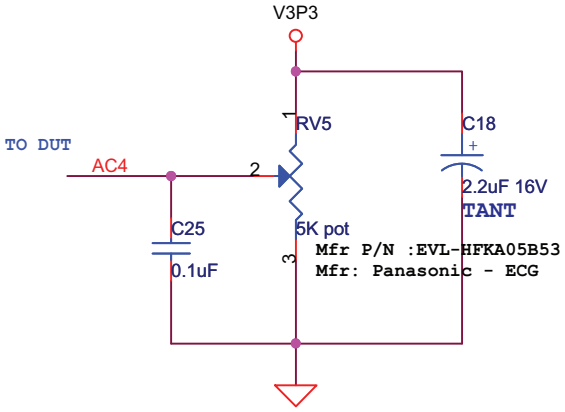
***Figure 8 •*** **PWM Circuit Schematic**




## 4.5.2 Potentiometer Circuit

A potentiometer circuit is provided on the Fusion Advanced Development Kit to sweep voltage. The potentiometer circuit is connected to the AC input pin, which can be used to monitor voltage. One common application is to adjust the potentiometer and measure the voltage on the AC pin.

***Figure 9 •*** **Potentiometer Circuit Schematic**



## 4.5.3 Current Sensing Circuit

For current monitor applications, two current sensing circuits are provided on the Fusion Advanced Development Kit board. One of the current sensing circuits is for the 3.3 V voltage rail and the other is for the 1.5 V voltage rail (Figure 11, page 15) of the Fusion FPGA.

***Figure 10 •*** **Current Sensing Schematic (3.3 V)**

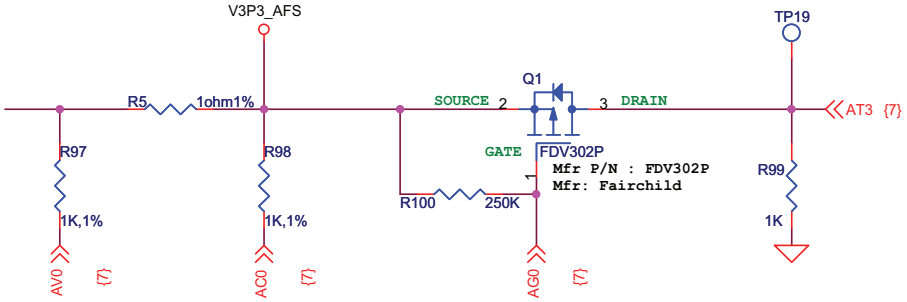
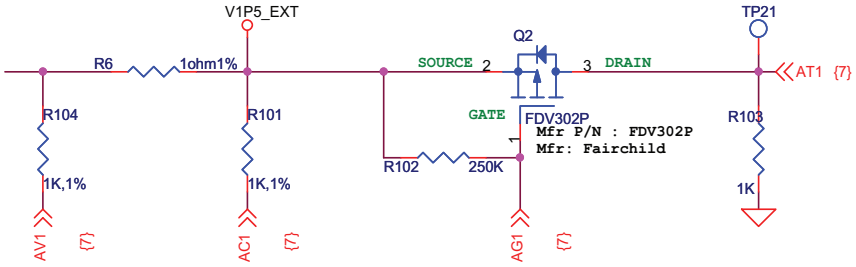


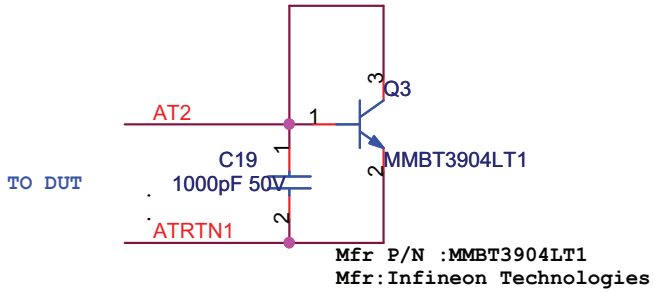

***Figure 11 •*** **Current Sensing Schematic (1.5 V)**




## 4.5.4 Temperature Monitor Diode

One external temperature diode on the Fusion Advanced Development Kit board is available for temperature measurement. This temperature diode is routed to the analog temperature (AT) and AT return (ATRTN) input pins of the temperature monitor block.

***Figure 12 •*** **Temperature Diode Schematic**



## 4.5.5 MOSFET for the Gate Driver Block

Two external p-channel MOSFETs are populated on the board, connected to the AG pins of the Fusion Analog Quad. One MOSFET is connected on the 3.3 V voltage rail and the other is on the 1.5 V voltage rail of the Fusion FPGA (Figure 14, page 16). The output of these MOSFETs goes to the AT pads, which can be set to monitor voltage. These MOSFETs can be used for a variety of voltage sequencing applications.

***Figure 13 •*** **MOSFET Schematic (3.3 V)**

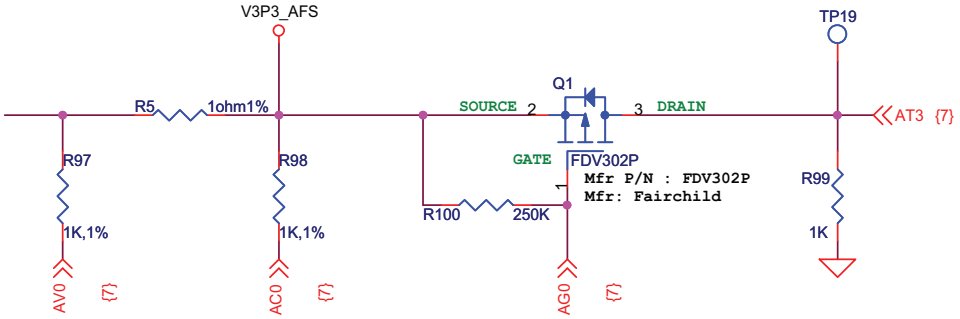
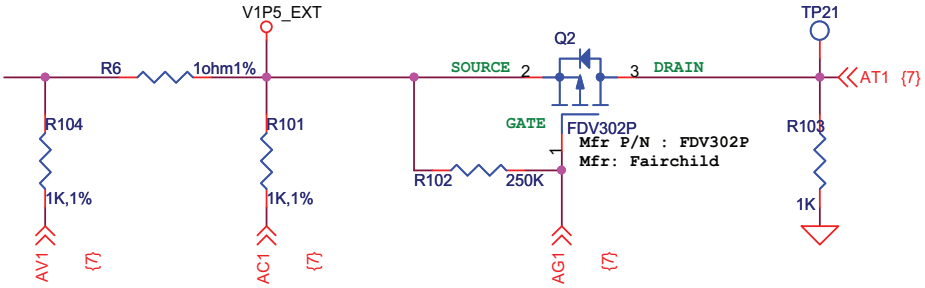


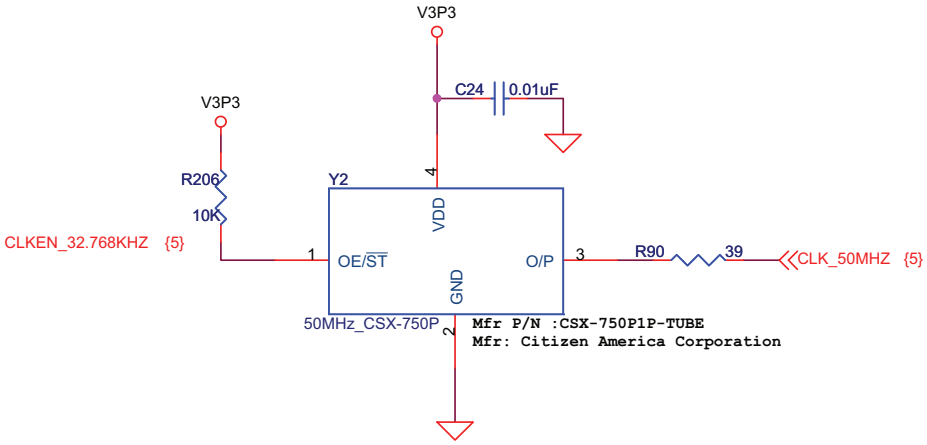

***Figure 14 •*** **MOSFET Schematic (1.5 V)**




## 4.5.6 Clock Oscillator

A 50 MHz clock oscillator with 50 ppm is available on the board. This clock oscillator is connected to the FPGA to provide a system or reference clock. An on-chip Fusion PLL can be configured and instantiated in the FPGA to generate a wide range of high-precision clock frequencies.

***Figure 15 •*** **Clock Oscillator Schematic**



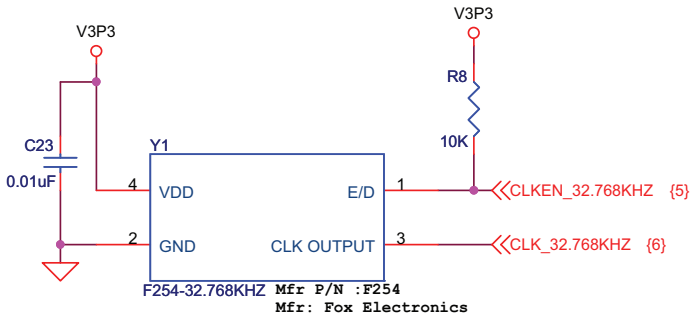

## 4.5.7 Crystal Oscillator

A 32.768 KHz off-chip crystal oscillator with 50 ppm is populated on the board. The off-chip crystal oscillator is connected to the digital XTAL1 and XTAL2 (on-chip crystal oscillator) inputs of the Fusion FPGA. The on-chip crystal oscillator circuit works with the low frequency the off-chip crystal to generate a

high-precision clock. It has an accuracy of 100 ppm (0.01%) and is capable of providing system clocks for Fusion peripherals and other system clock networks, both on-chip and off-chip. When combined with the Fusion on-chip CCC/PLL blocks, a wide range of clock frequencies can be created to support various design requirements. In addition, a Fusion programmable real-time counter (RTC), clocked by the on-chip crystal oscillator, provides power sequencing and voltage regulator control. Refer to the *Fusion and Extended Temperature Fusion FPGA Fabric User Guide* for additional details on these clocking resources.

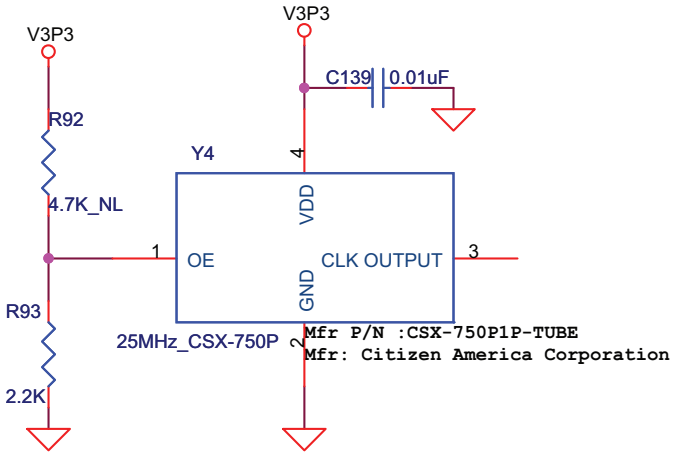
A sample clocking option utilizing the on- and off-chip crystal oscillator for a Fusion FPGA is shown in the following figure.

***Figure 16 •*** **Fusion Clock Options**




The following figure shows the schematic for the 25 MHz off-chip crystal oscillator.

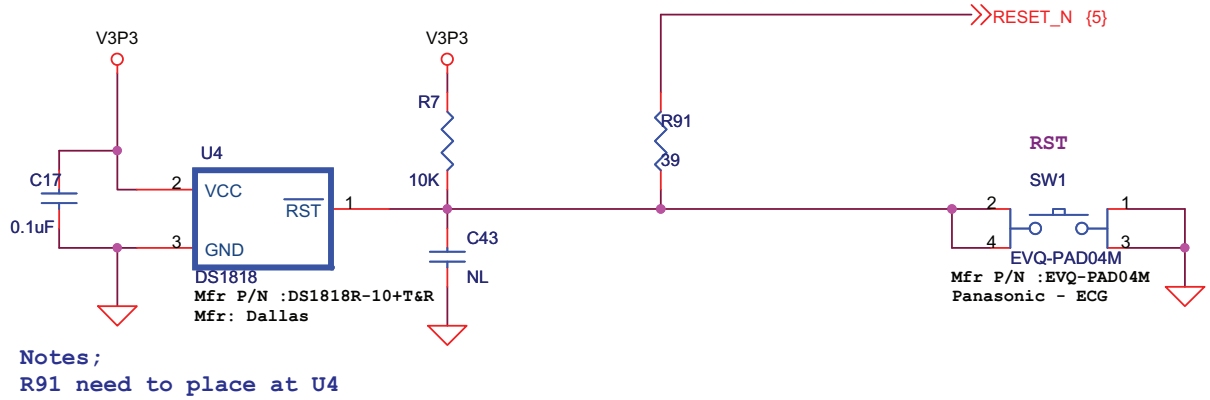
***Figure 17 •*** **25 MHz Off-Chip Crystal Oscillator Schematic**



## 4.5.8 Push-Button System Reset

A push-button system reset switch with a Schmitt trigger is provided on the board. The Schmitt trigger reduces noise on the system reset push-button.

***Figure 18 •*** **Push-Button System Reset Schematic**




## 4.5.9 Push-Button Switches and User LEDs

Push-button switches and user LEDs can also be used for debug and for various applications, such as gaming.

***Figure 19 •*** **Test and Navigation Switches**

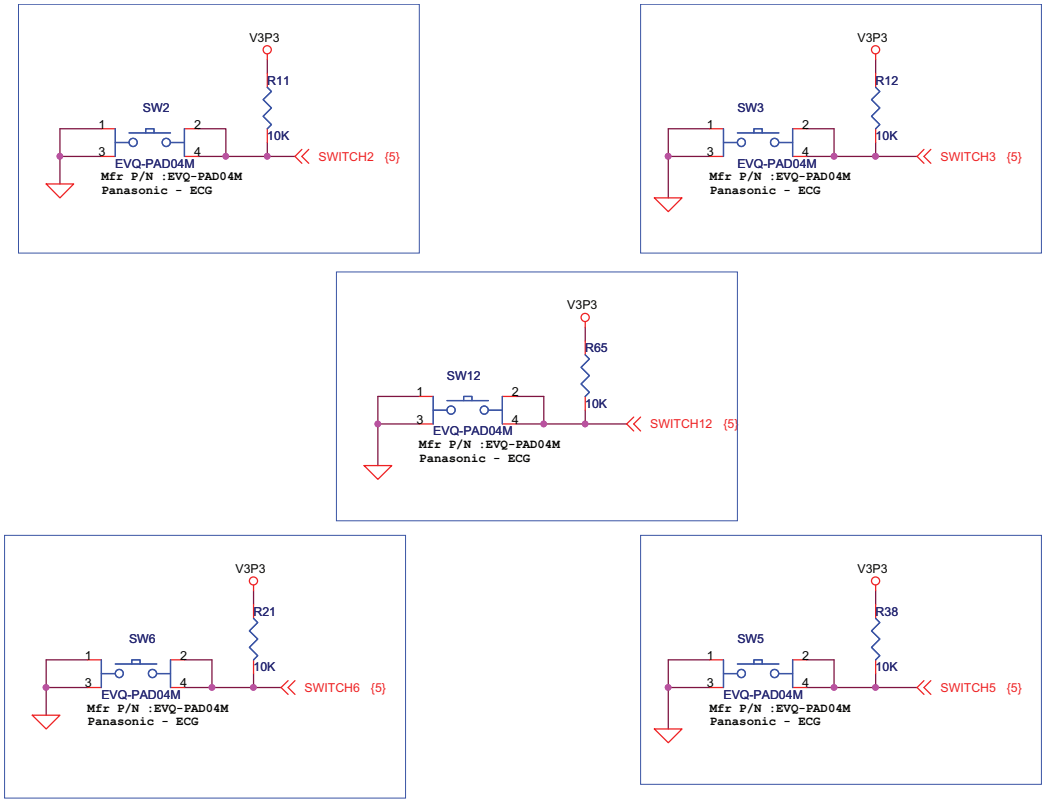
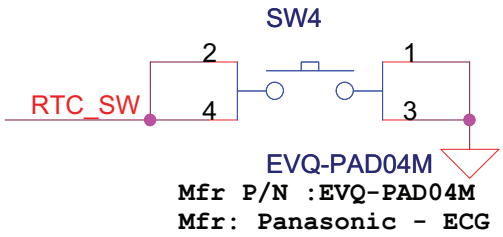


***Figure 20 •*** **Push-Button Switch for PUB**




The FADK also contains a 8-position DIP switch bank and a 12-LED module (Figure 22, page 19) for general purpose use. All signals are connected to the FPGA. The LEDs and switches are active High and the switches have 10-K pull-down resistors. You can also utilize any unused debug pins available.

***Figure 21 •*** **DIP Switch Schematic**

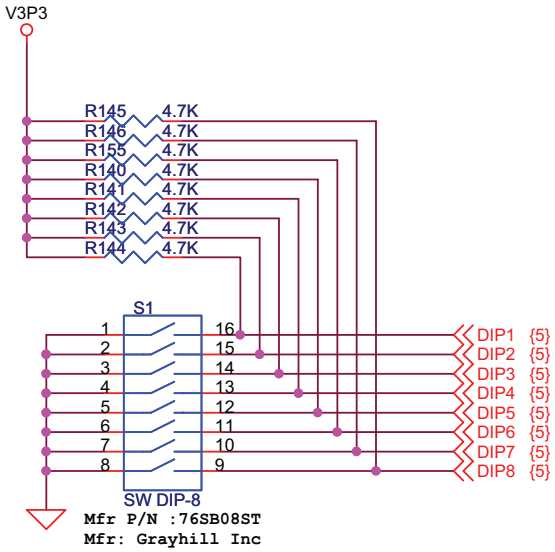
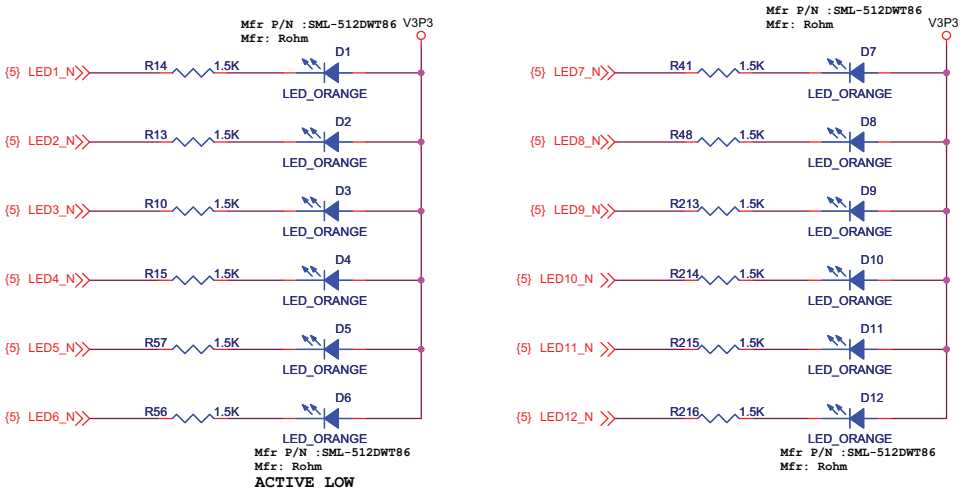



***Figure 22 •*** **LEDs Schematic**



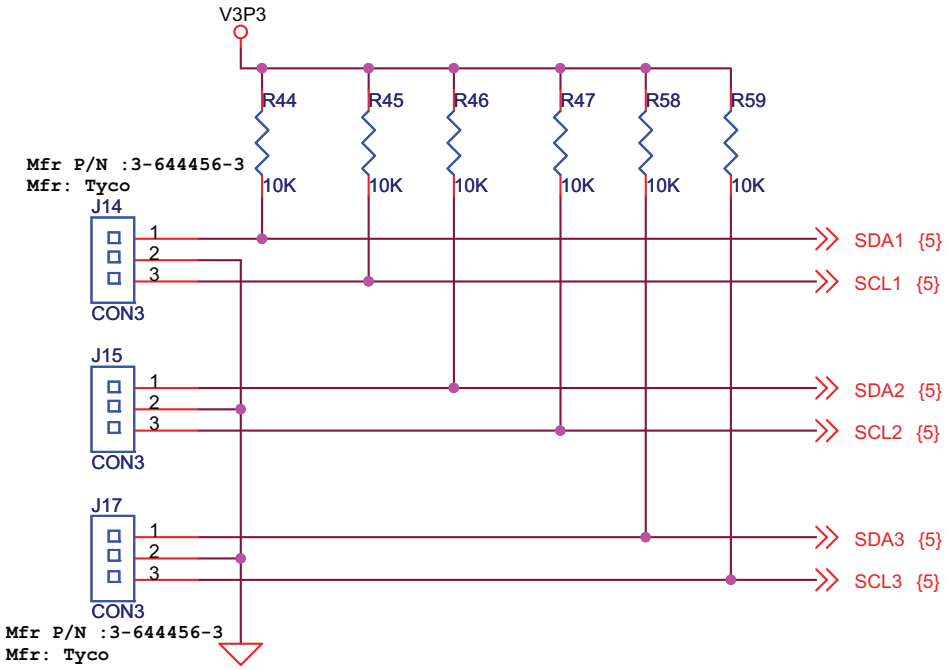

## 4.5.10 I2C Interface

Three inter-integrated circuit (I2C) headers with pull-up resistors—J14, J15, and J17 (Figure 23, page 20)—are provided on-board to showcase the I2C capabilities of this development kit. These

standard I2C interface signals are directly connected to the Fusion FPGA and can extend the capabilities of this embedded system.

Any standard I2C controller can be implemented or instantiated in the Fusion FPGA to allow communication with the I2C interface. In addition, the Microsemi IP catalog includes various programmable I2C controllers, specifically CoreI2C, with an APB interface that can be instantiated in the FPGA design with a Cortex-M1 embedded processor. The CoreI2C controller supports both Master and Slave modes with configurable parameters for various applications. The board is populated with an OLED display with I2C interfaces so you can evaluate the ability of the M1-enabled Fusion advanced system to communicate with an I2C device on this development kit.

***Figure 23 •*** **I2C Interface Schematic**

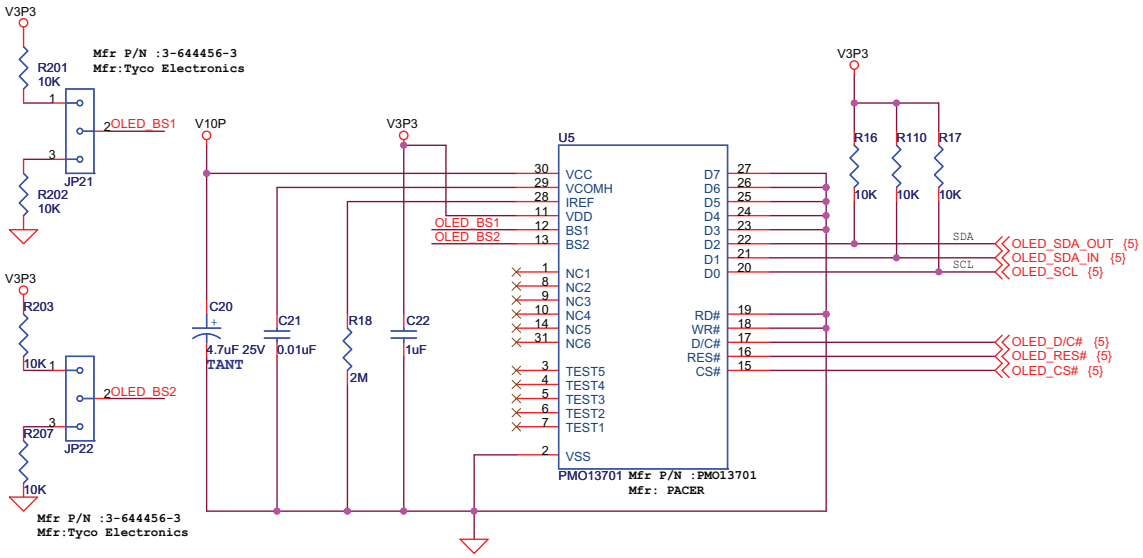



## 4.5.11 OLED Display

A 96×16-pixel low-power OLED is available on the board for display. This low-power device, BLUE OLED, requires 3.3 V and 10 V power supplies. By default, the OLED supports the I2C, but it can also support an SPI Interface. Table 11, page 21 lists the configuration for the I2C and the SPI interfaces. The OLED displays sharp gaming images or text. For example, the Fusion FPGA RTC current time or time between two events can be displayed on the OLED.

**Note:** The latest revision of Fusion Advanced Development kit (M1AFS-ADV-DEV-KIT-PWR-2) does not contain OLED display on the board.

***Figure 24 •*** **OLED Display Schematic**




The default connection for JP21 and JP22 is 1–2.

***Table 11 •*** **OLED Configuration Table**

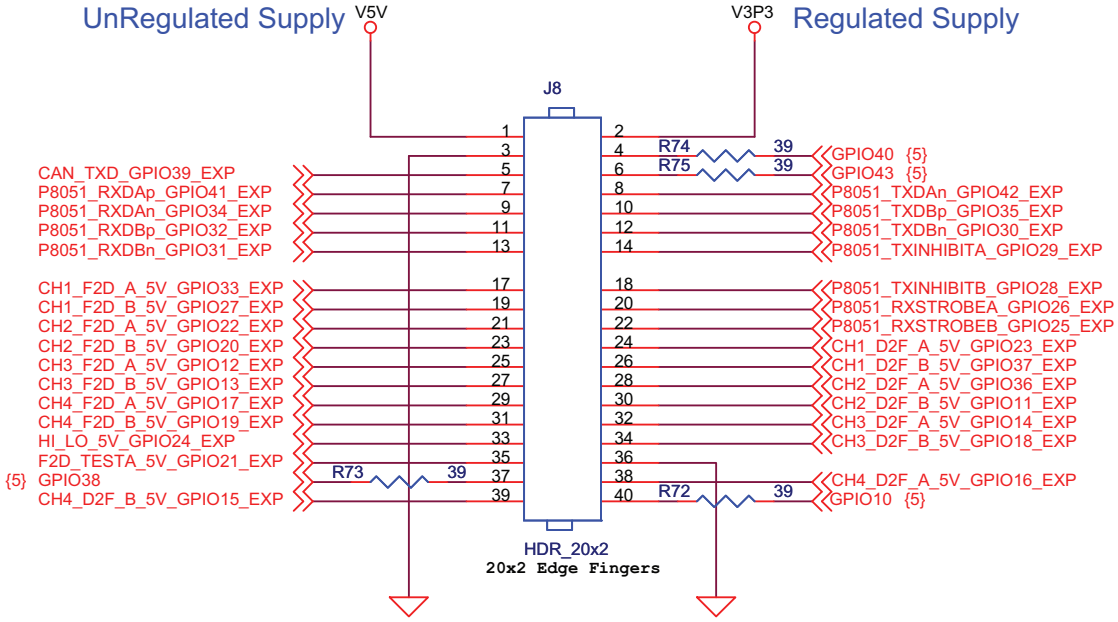
| | I2C Interface | SPI Interface |
|---|---|---|
| BS1 | 1 | 0 |
| BS2 | 0 | 0 |

## 4.5.12 Interface Connector

A standard interface connector on the board can be used to extend this development kit to connect with additional daughter cards, some of which are developed by partners and third party vendors. The interface possibilities are numerous, such as flash and SRAM memory interfaces, keyboard (HMI) interfaces, LCD interfaces, and motor control interfaces.

**CAUTION**: I/Os on this connector are shared between this connector and the 44-pin legacy connector. Only one daughter board can be connected at a time.

***Figure 25 •*** **Interface Connector Schematic**



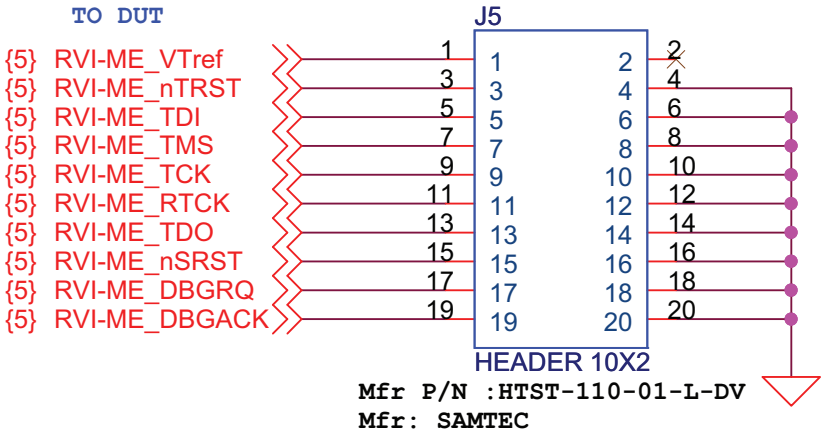

**Note:** Mating Connector – Mating Connector Part Number: MEC1-120-02-F-S-EM2 (Manufacturer: Samtec) Pin No:15 & 16 Should be NC For Mating Connector Polarized Pins
LAYOUT NOTE: R72, R73, R74, R75 SHOULD BE PLACED NEAR THE DUT.

**Note:** To design new interfaces on this connector, run a complete power analysis of your design to check for the available power budget.

## 4.5.13 RealView Header

One 10×2 RealView Header is provided on the board for debugging. This header allows RealView software development tools to easily debug or configure the embedded Cortex-M1 processor during board bring-up.

***Figure 26 •*** **RealView Header Schematic**




## 4.5.14 Ethernet Interface

One Ethernet interface, configured for MII Full Duplex mode, and a low-power 10/100 Mbps single-port Ethernet physical layer transceiver (U10) are provided on-board (Figure 28, page 24). The Ethernet physical layer features integrated sub-layers to support both 10BASE-T and 100BASE-TX Ethernet protocols. These sub-layers ensure compatibility and interoperability with many other standards-based Ethernet solutions.

Two LEDs are populated on the board for this ethernet interface. One is for speed and the other is for activity.

The Ethernet RJ45 interface and physical layer, along with an Ethernet Media Access Controller (MAC) that can be programmed onto the M1-enabled Fusion FPGA, serves many purposes. For example, this interface can be used to access the Fusion FPGA to monitor the ADC data over a network. The embedded system memory and control registers can be accessed and processed remotely to support system management. The Microsemi IP catalog includes a Core10100 Ethernet MAC with Host Controller.

***Figure 27 •*** **Typical Application**

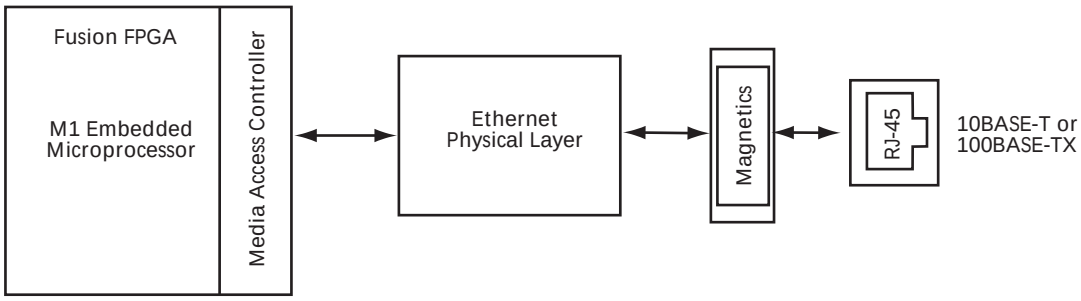
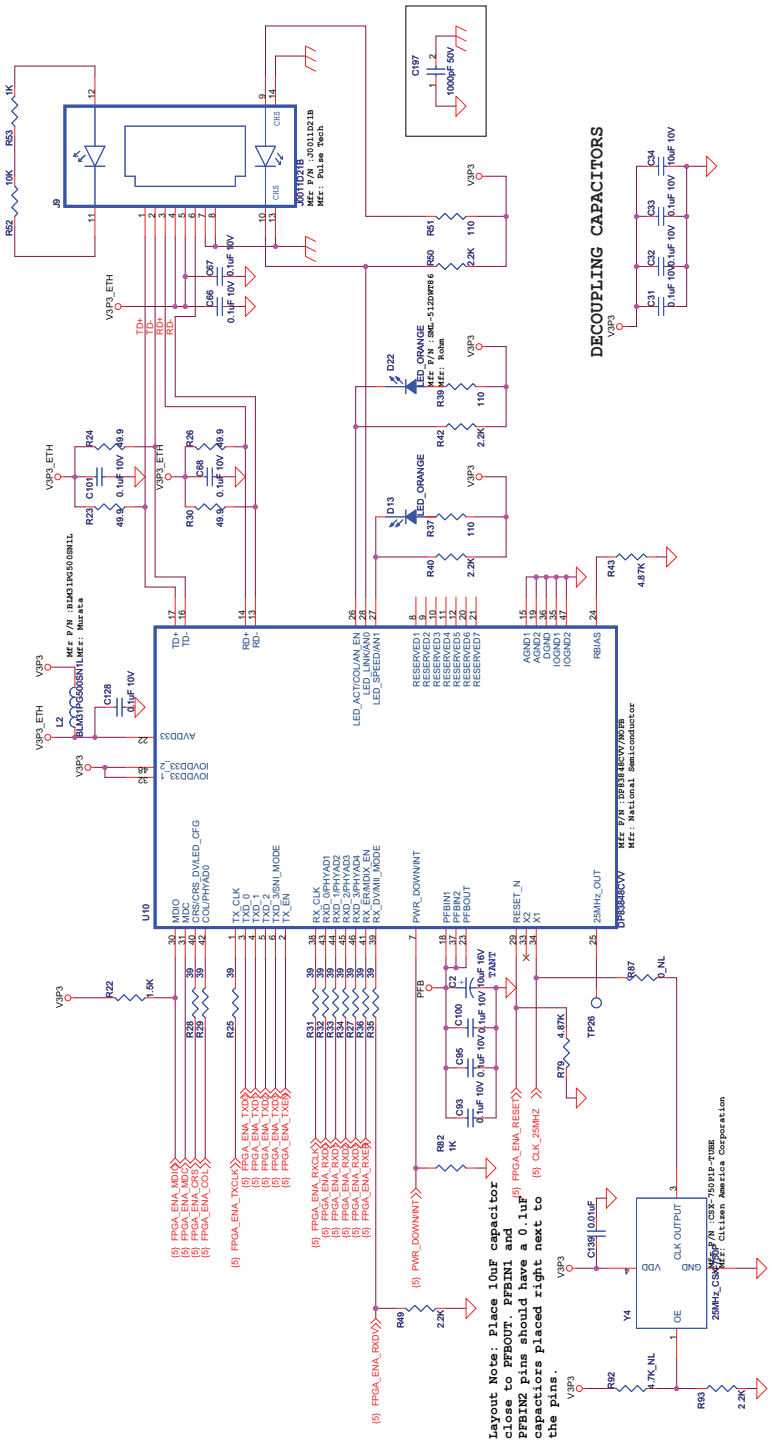


***Figure 28 •*** **Ethernet Interface Schematic**



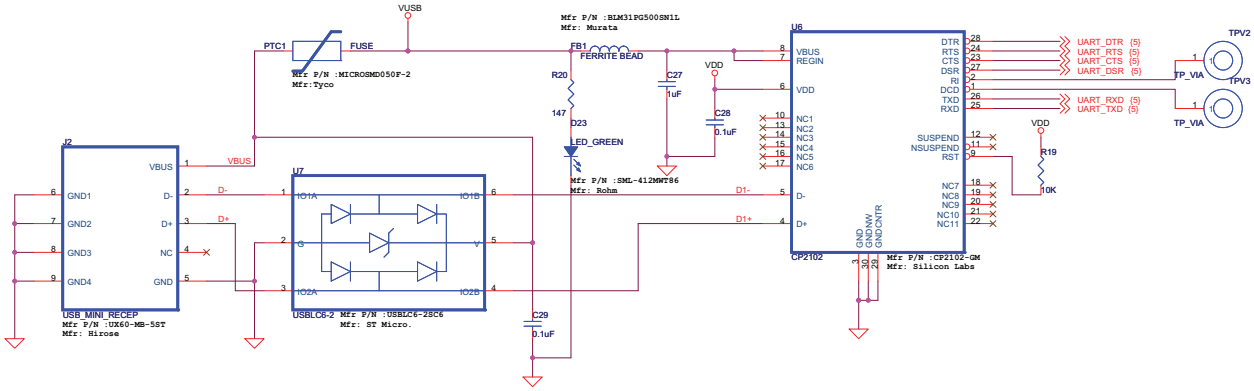

## 4.5.15 USB-to-UART Interface

Included on the evaluation board is a USB-to-UART interface with ESD protection. This interface includes an integrated USB-to-UART bridge controller (U6) to provide a standard UART connection with the Fusion FPGA. Any standard UART controller can be implemented in the Fusion FPGA to allow access with this interface. In addition, the Microsemi IP catalog includes various UART controllers, specifically CoreUARTapb, with an AMBA APB interface that can be instantiated in the FPGA with a

Cortex-M1 embedded processor. The programmable CoreUARTapb controller supports both asynchronous and synchronous modes with configurable parameters for various applications.

One application of the USB-to-UART interface is to allow HyperTerminal on a PC to communicate with the Fusion FPGA. HyperTerminal is a serial communications application program that can be installed in the Windows operating system. A basic HyperTerminal program is usually distributed with Windows. With a USB driver properly installed, and the correct COM port and communication settings selected, you can use the HyperTerminal program to communicate with a design running on the Fusion FPGA device.

***Figure 29 •*** **USB-to-UART Interface Schematic**

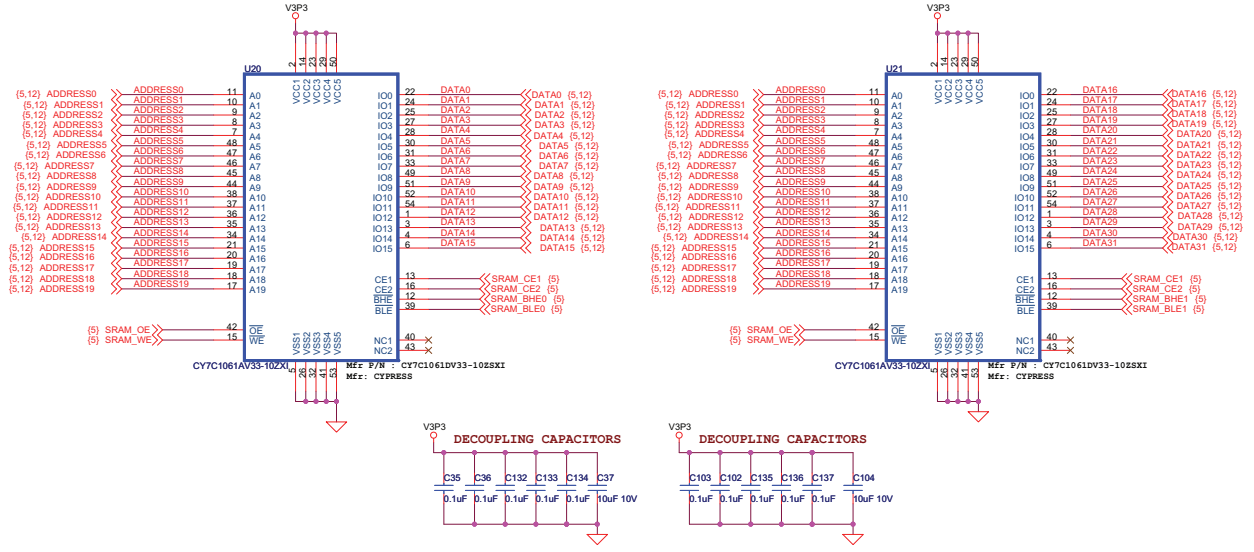



## 4.5.16 SRAM Components

Two SRAM components are provided on this M1-embedded Fusion Advanced Development Kit board, totaling 4 MBytes of memory. Each SRAM has a 16-bit data bus interface, resulting in a 32-bit data bus. In addition to the embedded Flash memory in the Fusion FPGA, these on-board SRAMs extend the memory space of the system and can be easily accessed by an embedded processor, such as Cortex-M1.

In a embedded processor system, these on-board SRAM can be accessed by a standard memory controller, such as CoreMemCtrl (available from Microsemi's IP catalog).

***Figure 30 •*** **SRAM Components Schematic**

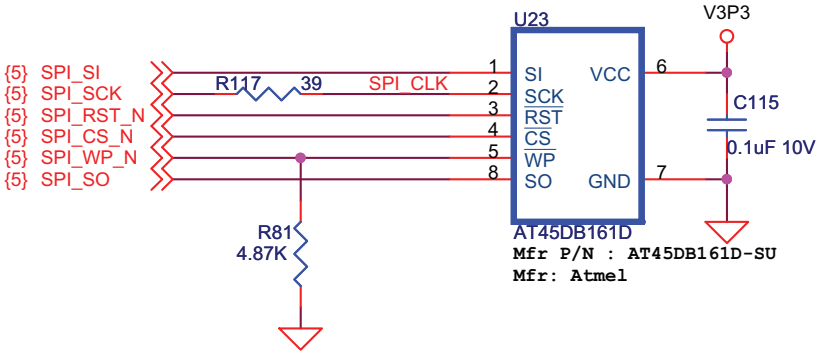



## 4.5.17 SPI Flash

One 2-MByte flash memory with SPI interface is available on the board and can be used by an embedded CoreABC or a Cortex-M1 embedded microprocessor to access additional memory off-chip. The flash interface, serial peripheral interface (SPI), is a synchronous serial data link standard. In an

embedded microprocessor system, CoreSPI (available from Microsemi's IP catalog) can be instantiated to communicate with the SPI flash. Some advantages of the SPI interface are full duplex communication and higher throughput than I2C.

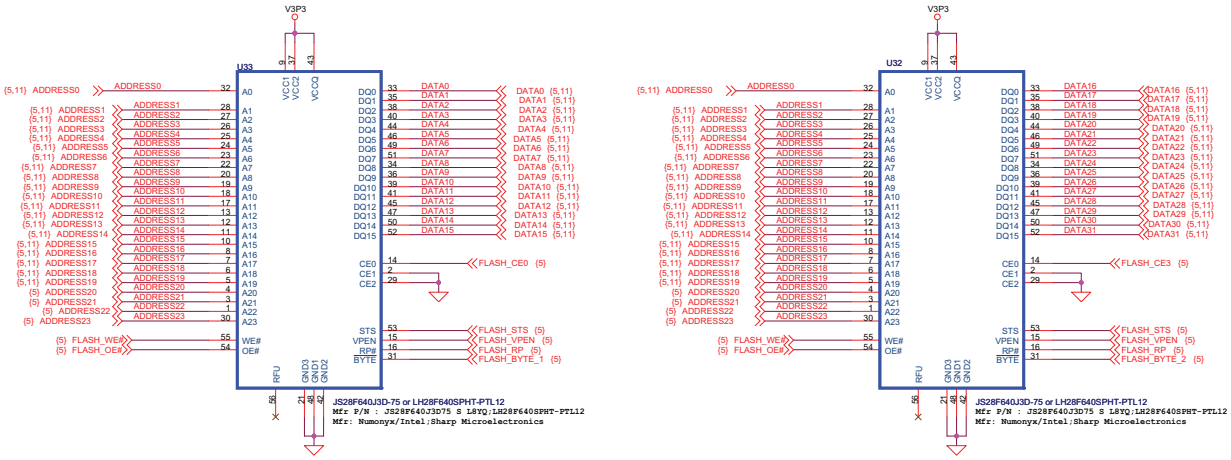
***Figure 31 •*** **SPI Flash Schematic**




## 4.5.18 Parallel Flash

Two 32-MByte parallel flash memories are available on the board, totaling 64 MBytes of parallel flash memory. Each flash has a 16-bit data bus, resulting in a 32-bit data bus.

***Figure 32 •*** **Parallel Flash Components Schematic**




## 4.5.19 DirectC Programming

There is not a ProASIC3-based FlashPro3 connector on the board; instead a standard FlashPro3 10-pin connector is provided. This interfaces with 5 GPIOs and follows same pinout as FlashPro3. This can be used to program an Microsemi FPGA on another board.

***Figure 33 •*** **DirectC Programming of Another Board**

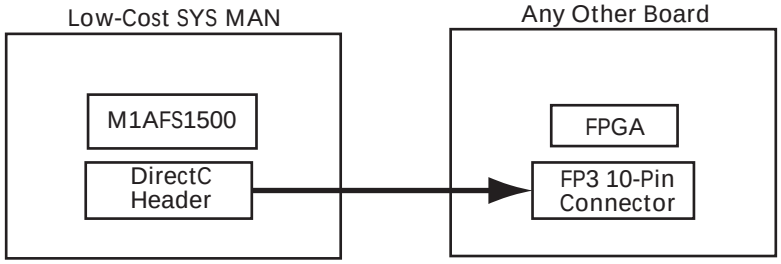
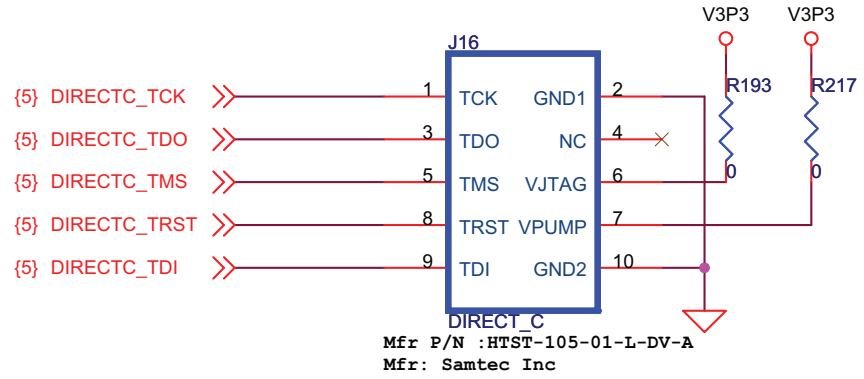


***Figure 34 •*** **DirectC Header Schematic**




The following table lists the configuration details for the target board.

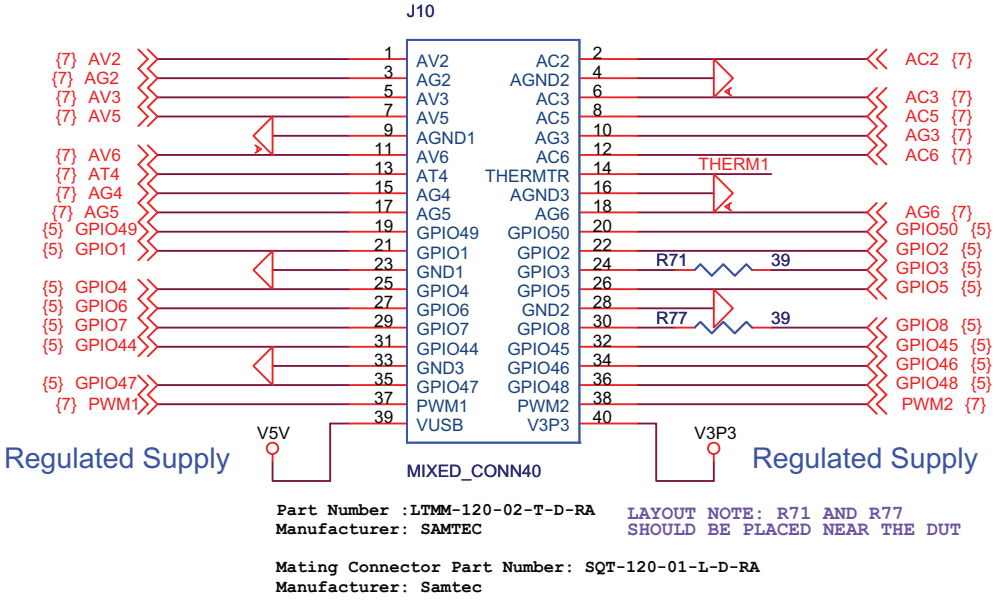
***Table 12 •*** **VPUMP/VJTAG Configuration on Target Board**

| VPUMP/VJTAG Configuration | R193 | R217 |
|---|---|---|
| Connected to 3.3 V | Do not populate | Do not populate |
| Not connected (powers through FP3) | Populate | Populate |

## 4.5.20 Mixed-Signal Header

A range of Fusion mixed-signal pins, particularly the analog AV, AC, AG, and AT pins of the Analog Quad and GPIO I/O pins, is available on the mixed-signal header on this board. This header can be used by various daughter boards to access the Fusion analog pins to demonstrate various applications, such as motor control, touch screen, and voltage trimming.

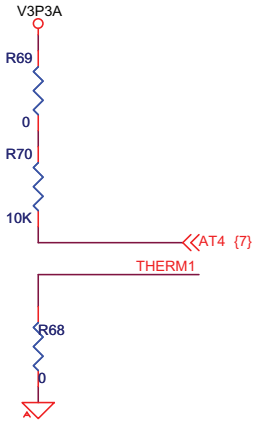
***Figure 35 •*** **Mixed-Signal Header Schematic**




**Note:** To design new interfaces on this connector, run a complete power analysis of your design to check for the available power budget.

A thermistor circuit is available to use with the mixed-signal header for temperature monitor applications.

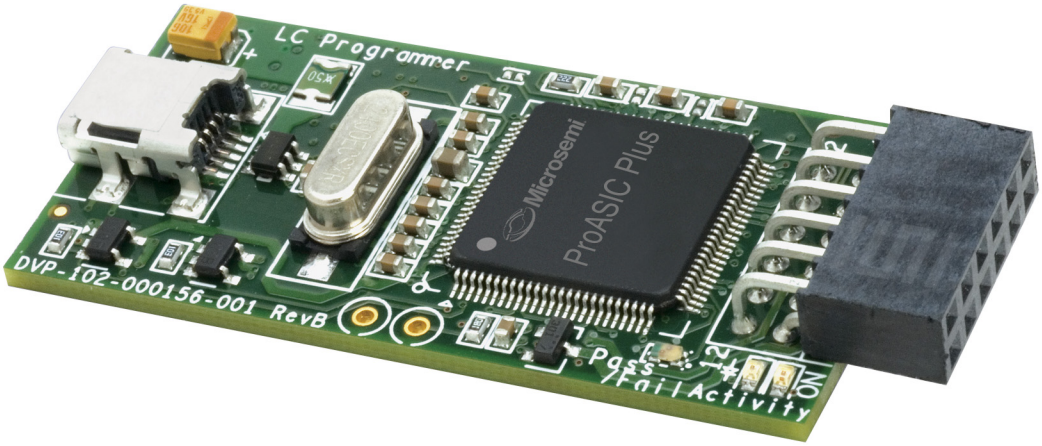
***Figure 36 •*** **Thermistor Schematic**




## 4.6 Low-Cost Programming Stick

The Fusion Advanced Development Kit board can be programmed using the low-cost programming stick (LCPS). The LCPS is a special version of the FlashPro3 programming circuitry that is compatible with FlashPro3 and the generic FlashPro programming software.

***Figure 37 •*** **Low-Cost Programming Stick**




**Note:** The LCPS supplied with this kit is intended for use with the Fusion Advanced Development Kit. An LCPS supplied for other kits, although electrically and functionally equivalent, may not connect seamlessly with the Fusion Advanced Development Kit board.

The LCPS, like this Fusion Advanced Development Kit board, is RoHS-compliant and is completely lead (Pb) free. To use the LCPS with the FlashPro software, select the FlashPro3 from the list of programmer types. The LCPS behaves exactly as if it were a regular encased FlashPro3 programmer. The 12-pin female connector socket is designed to interface to the 12-pin right-angle male header on the Fusion Advanced Development Kit board.

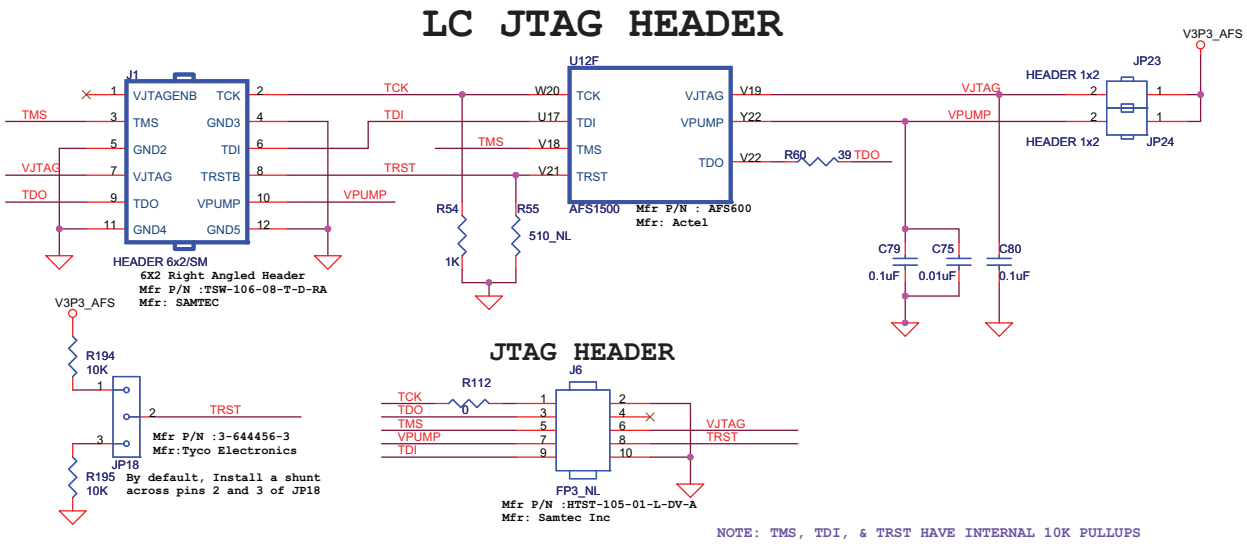
You do not need to have the LCPS connected to the Fusion Advanced Development Kit board to operate once the FPGA has been programmed. The Fusion Advanced Development Kit board requires the LCPS connected only during programming.

The LCPS programs the FPGA through the JTAG pins. Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). $V_{CC}$ must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; $V_{JTAG}$ alone is insufficient. Both $V_{JTAG}$ and $V_{CC}$ to the Fusion part must be supplied to allow JTAG signals to

transition the Fusion device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the $V_{JTAG}$ pin together with the TRST pin could be tied to GND.

The JTAG Header schematics is shown in the following figure.

***Figure 38 •*** **JTAG Header Schematic for LCPS Connection**



# 5 Pin List

The following table lists the Fusion M1AFS1500 pin list and I/O pins connections.

***Table 13 •*** **FPGA Pin List**

| M1AFS1500 Pin Number | M1AFS1500 Pin Name | Board Signal Name |
|---|---|---|
| E19 | IO49PDB2V0 | ADDRESS0 |
| E22 | GBC2/IO46PDB2V0 | ADDRESS1 |
| F20 | IO50PDB2V0 | ADDRESS2 |
| F21 | IO50NDB2V0 | ADDRESS3 |
| F22 | IO51PDB2V0 | ADDRESS4 |
| B18 | GBA1/IO42PDB1V2 | ADDRESS5 |
| B17 | GBC1/IO40PDB1V2 | ADDRESS6 |
| C16 | IO37NDB1V2 | ADDRESS7 |
| B15 | IO31PDB1V1 | ADDRESS8 |
| B14 | IO31NDB1V1 | ADDRESS9 |
| C22 | GBB2/IO45PDB2V0 | ADDRESS10 |
| C21 | IO48PSB2V0 | ADDRESS11 |
| A18 | GBA0/IO42NDB1V2 | ADDRESS12 |
| A17 | GBC0/IO40NDB1V2 | ADDRESS13 |
| A16 | IO35PDB1V2 | ADDRESS14 |
| B12 | IO26NDB1V0 | ADDRESS15 |
| A12 | IO26PDB1V0 | ADDRESS16 |
| A13 | IO27NDB1V1 | ADDRESS17 |
| A14 | IO27PDB1V1 | ADDRESS18 |
| A15 | IO35NDB1V2 | ADDRESS19 |
| C14 | IO29PDB1V1 | ADDRESS20 |
| C13 | IO29NDB1V1 | ADDRESS21 |
| D12 | IO23PDB1V0 | ADDRESS22 |
| J7 | IO111PDB4V0 | ADDRESS23 |
| D19 | IO47PPB2V0 | DATA0 |
| D17 | GBB1/IO41PDB1V2 | DATA1 |
| D16 | IO37PDB1V2 | DATA2 |
| G17 | IO53PDB2V0 | DATA3 |
| G16 | IO38PPB1V2 | DATA4 |
| E15 | IO36NPB1V2 | DATA5 |
| D14 | IO34NDB1V1 | DATA6 |
| F14 | IO30PDB1V1 | DATA7 |
| E18 | IO47NPB2V0 | DATA8 |

*Table 13 •* **FPGA Pin List *(continued)***

| M1AFS1500 Pin Number | M1AFS1500 Pin Name | Board Signal Name |
|---|---|---|
| C17 | GBB0/IO41NDB1V2 | DATA9 |
| F17 | IO38NPB1V2 | DATA10 |
| F16 | IO36PPB1V2 | DATA11 |
| D15 | IO34PDB1V1 | DATA12 |
| G14 | IO28PDB1V1 | DATA13 |
| E14 | IO32PPB1V1 | DATA14 |
| F13 | IO30NDB1V1 | DATA15 |
| M21 | GCB0/IO63NDB2V0 | DATA16 |
| M18 | IO69NDB2V0 | DATA17 |
| L19 | GCA1/IO64PDB2V0 | DATA18 |
| L22 | GCC1/IO62PDB2V0 | DATA19 |
| K20 | IO61NDB2V0 | DATA20 |
| J21 | IO55PSB2V0 | DATA21 |
| K22 | IO56NDB2V0 | DATA22 |
| H21 | IO54NDB2V0 | DATA23 |
| M22 | GCB1/IO63PDB2V0 | DATA24 |
| M19 | GCA0/IO64NDB2V0 | DATA25 |
| L21 | GCC0/IO62NDB2V0 | DATA26 |
| K19 | IO68NPB2V0 | DATA27 |
| J22 | IO56PDB2V0 | DATA28 |
| J20 | GCC2/IO61PDB2V0 | DATA29 |
| H22 | IO54PDB2V0 | DATA30 |
| G22 | IO51NDB2V0 | DATA31 |
| J2 | IO113NDB4V0 | LED1_N |
| J3 | GFB2/IO109PDB4V0 | LED2_N |
| J4 | GFA2/IO110PDB4V0 | LED3_N |
| M7 | GFB0/IO106NDB4V0 | LED4_N |
| K4 | IO110NDB4V0 | LED5_N |
| L5 | GFC1/IO107PDB4V0 | LED6_N |
| L7 | GFB1/IO106PDB4V0 | LED7_N |
| M5 | GFC0/IO107NDB4V0 | LED8_N |
| H1 | IO115NDB4V0 | LED9_N |
| G19 | IO52PDB2V0 | LED10_N |
| M16 | IO70NDB2V0 | LED11_N |
| W19 | IO68PPB2V0 | LED12_N |
| D3 | IO123NDB4V0 | DIRECTC_TDI |
| H5 | IO114PDB4V0 | 10K to GND |
| B3 | GAA0/IO01NDB0V0 | CAN_RXD |

*Table 13 •* **FPGA Pin List *(continued)***

| M1AFS1500 Pin Number | M1AFS1500 Pin Name | Board Signal Name |
|---|---|---|
| A3 | GAA1/IO01PDB0V0 | CAN_TXD_GPIO39 |
| D6 | GAC0/IO03NDB0V0 | CH1_D2F_A_5V_GPIO23 |
| C6 | IO05NDB0V1 | CH1_D2F_B_5V_GPIO37 |
| D8 | IO10NDB0V1 | CH1_F2D_A_5V_GPIO33 |
| B8 | IO09NDB0V1 | CH1_F2D_B_5V_GPIO27 |
| B6 | IO04PDB0V0 | CH2_D2F_A_5V_GPIO36 |
| A6 | IO07NDB0V1 | CH2_D2F_B_5V_GPIO11 |
| A8 | IO09PDB0V1 | CH2_F2D_A_5V_GPIO22 |
| G9 | IO06NDB0V1 | CH2_F2D_B_5V_GPIO20 |
| D7 | GAC1/IO03PDB0V0 | CH3_D2F_A_5V_GPIO14 |
| C7 | IO05PDB0V1 | CH3_D2F_B_5V_GPIO18 |
| E9 | IO08PDB0V1 | CH3_F2D_A_5V_GPIO12 |
| F9 | IO12NDB0V1 | CH3_F2D_B_5V_GPIO13 |
| A7 | IO07PDB0V1 | CH4_D2F_A_5V_GPIO16 |
| E8 | IO08NDB0V1 | CH4_D2F_B_5V_GPIO15 |
| C9 | IO11NDB0V1 | CH4_F2D_A_5V_GPIO17 |
| A9 | IO13NDB0V2 | CH4_F2D_B_5V_GPIO19 |
| J16 | GCB2/IO60PDB2V0 | CLK_50MHZ |
| G1 | IO115PDB4V0 | CLKEN_32.768KHZ |
| K6 | IO104NDB4V0 | DIG_1 |
| K7 | IO111NDB4V0 | DIG_2 |
| R2 | IO102NDB4V0 | DIP1 |
| P1 | GFA1/IO105PDB4V0 | DIP2 |
| P2 | GFA0/IO105NDB4V0 | DIP3 |
| L1 | IO108NDB4V0 | DIP4 |
| K1 | GFC2/IO108PDB4V0 | DIP5 |
| R1 | IO102PDB4V0 | DIP6 |
| N3 | IO101PDB4V0 | DIP7 |
| K3 | IO109NDB4V0 | DIP8 |
| C4 | IO00PDB0V0 | DIRECTC_TCK |
| C3 | IO00NDB0V0 | DIRECTC_TDO |
| D5 | GAA2/IO125PDB4V0 | DIRECTC_TMS |
| D4 | GAC2/IO123PDB4V0 | DIRECTC_TRST |
| W5 | IO86NDB4V0 | Ethernet CLK |
| C10 | IO14PDB0V2 | F2D_TESTA_5V_GPIO21 |
| D22 | IO45NDB2V0 | F2D_TESTB_5V |
| F19 | IO49NDB2V0 | FLASH_BYTE_1 |
| L18 | IO69PDB2V0 | FLASH_BYTE_2 |

*Table 13 •* **FPGA Pin List *(continued)***

| M1AFS1500 Pin Number | M1AFS1500 Pin Name | Board Signal Name |
|---|---|---|
| K17 | IO58PDB2V0 | FLASH_CE0 |
| L16 | IO70PDB2V0 | FLASH_CE3 |
| G13 | IO28NDB1V1 | FLASH_OE# |
| H17 | IO53NDB2V0 | FLASH_RP |
| D13 | IO32NPB1V1 | FLASH_STS |
| J17 | IO58NDB2V0 | FLASH_VPEN |
| E12 | IO22PDB1V0 | FLASH_WE# |
| AB3 | IO94NSB4V0 | FPGA_ENA_COL |
| Y2 | IO87NDB4V0 | FPGA_ENA_CRS |
| W1 | IO93PDB4V0 | FPGA_ENA_MDC |
| R4 | IO91PDB4V0 | FPGA_ENA_MDIO |
| P5 | IO96NDB4V0 | FPGA_ENA_RESET |
| Y4 | IO85NDB4V0 | FPGA_ENA_RXCLK |
| W4 | GEB2/IO86PDB4V0 | FPGA_ENA_RXD0 |
| W3 | IO93NDB4V0 | FPGA_ENA_RXD1 |
| V4 | GEA1/IO88PDB4V0 | FPGA_ENA_RXD2 |
| V2 | GEB0/IO89NDB4V0 | FPGA_ENA_RXD3 |
| Y3 | GEA2/IO85PDB4V0 | FPGA_ENA_RXDV |
| Y1 | GEC2/IO87PDB4V0 | FPGA_ENA_RXER |
| V1 | GEB1/IO89PDB4V0 | FPGA_ENA_TXCLK |
| U3 | GEC1/IO90PDB4V0 | FPGA_ENA_TXD0 |
| U2 | IO98NDB4V0 | FPGA_ENA_TXD1 |
| U1 | IO98PDB4V0 | FPGA_ENA_TXD2 |
| T4 | IO95NDB4V0 | FPGA_ENA_TXD3 |
| U4 | GEC0/IO90NDB4V0 | FPGA_ENA_TXEN |
| U19 | IO84NDB2V0 | GPIO1 |
| C20 | GBA2/IO44PDB2V0 | GPIO10 |
| R17 | IO74NDB2V0 | GPIO2 |
| T17 | IO74PDB2V0 | GPIO3 |
| A20 | IO43PDB1V2 | GPIO38 |
| U20 | GDC2/IO84PDB2V0 | GPIO4 |
| D20 | IO44NDB2V0 | GPIO40 |
| A19 | IO43NDB1V2 | GPIO43 |
| T22 | GDC1/IO79PDB2V0 | GPIO44 |
| T19 | IO82NDB2V0 | GPIO45 |
| T20 | GDA2/IO82PDB2V0 | GPIO46 |
| R22 | IO75PDB2V0 | GPIO47 |
| R21 | IO75NDB2V0 | GPIO48 |

*Table 13 •* **FPGA Pin List *(continued)***

| M1AFS1500 Pin Number | M1AFS1500 Pin Name | Board Signal Name |
|---|---|---|
| W22 | IO76PPB2V0 | GPIO49 |
| R18 | GDA0/IO81NDB2V0 | GPIO5 |
| T16 | IO77PPB2V0 | GPIO50 |
| U21 | IO77NPB2V0 | GPIO6 |
| U22 | GDC0/IO79NDB2V0 | GPIO7 |
| R19 | GDB0/IO80NDB2V0 | GPIO8 |
| F10 | IO12PDB0V1 | HI_LO_5V_GPIO24 |
| R6 | IO92PDB4V0 | MPM_REG1_EN |
| P6 | IO99NDB4V0 | MPM_REG1_PWM |
| R5 | IO91NDB4V0 | MPM_REG2_EN |
| V5 | GEA0/IO88NDB4V0 | MPM_REG2_PWM |
| T1 | IO100PPB4V0 | MPM_REG3_EN |
| AB20 | IO76NPB2V0 | MPM_REG3_PWM |
| P7 | IO97NDB4V0 | MPM_REG4_EN |
| N7 | IO97PDB4V0 | MPM_REG4_PWM |
| A5 | GAB1/IO02PDB0V0 | OLED_CS# |
| G11 | IO16NDB0V2 | OLED_D/C# |
| G4 | IO116PDB4V0 | OLED_RES# |
| G3 | IO116NDB4V0 | OLED_SCL |
| F2 | IO118PDB4V0 | OLED_SDA_IN |
| F1 | IO118NDB4V0 | OLED_SDA_OUT |
| G12 | IO16PDB0V2 | P8051_RXDAn_GPIO34 |
| A4 | GAB0/IO02NDB0V0 | P8051_RXDAp_GPIO41 |
| D11 | IO23NDB1V0 | P8051_RXDBn_GPIO31 |
| A11 | IO24PDB1V0 | P8051_RXDBp_GPIO32 |
| B9 | IO11PDB0V1 | P8051_RXSTROBEA_GPIO26 |
| D9 | IO10PDB0V1 | P8051_RXSTROBEB_GPIO25 |
| B11 | IO24NDB1V0 | P8051_TXDAn_GPIO42 |
| B5 | IO04NDB0V0 | P8051_TXDAp |
| A10 | IO13PDB0V2 | P8051_TXDBn_GPIO30 |
| E11 | IO22NDB1V0 | P8051_TXDBp_GPIO35 |
| D10 | IO14NDB0V2 | P8051_TXINHIBITA_GPIO29 |
| G10 | IO06PDB0V1 | P8051_TXINHIBITB_GPIO28 |
| T3 | IO95PDB4V0 | PWR_DOWN/INT |
| H19 | GCA2/IO59PDB2V0 | RESET_N |
| P16 | IO83NDB2V0 | RVI-ME_DBGACK |
| P17 | IO78NDB2V0 | RVI-ME_DBGRQ |
| P18 | GDA1/IO81PDB2V0 | RVI-ME_nSRST |

*Table 13 •* **FPGA Pin List *(continued)***

| M1AFS1500 Pin Number | M1AFS1500 Pin Name | Board Signal Name |
|---|---|---|
| P21 | IO73PDB2V0 | RVI-ME_nTRST |
| N16 | GDB2/IO83PDB2V0 | RVI-ME_RTCK |
| N17 | IO78PDB2V0 | RVI-ME_TCK |
| P20 | IO73NDB2V0 | RVI-ME_TDI |
| P19 | GDB1/IO80PDB2V0 | RVI-ME_TDO |
| N19 | IO72NDB2V0 | RVI-ME_TMS |
| P22 | IO71NDB2V0 | RVI-ME_VTref |
| J5 | IO112NPB4V0 | SCL1 |
| T6 | IO92NDB4V0 | SCL2 |
| H6 | IO117NDB4V0 | SCL3 |
| J6 | IO104PDB4V0 | SDA1 |
| N6 | IO99PDB4V0 | SDA2 |
| G6 | IO117PDB4V0 | SDA3 |
| F3 | IO119NSB4V0 | SPI_CS_N |
| D1 | IO121NDB4V0 | SPI_RST_N |
| E2 | IO120PDB4V0 | SPI_SCK |
| E1 | IO120NDB4V0 | SPI_SI |
| C2 | IO122PSB4V0 | SPI_SO |
| C1 | IO121PDB4V0 | SPI_WP_N |
| G20 | IO52NDB2V0 | SRAM_BHE0 |
| N22 | IO71PDB2V0 | SRAM_BHE1 |
| J18 | IO57NDB2V0 | SRAM_BLE0 |
| N20 | IO72PDB2V0 | SRAM_BLE1 |
| J19 | IO59NDB2V0 | SRAM_CE1 |
| H18 | IO57PDB2V0 | SRAM_CE2 |
| K16 | IO60NDB2V0 | SRAM_OE |
| E21 | IO46NDB2V0 | SRAM_WE |
| E4 | GAB2/IO124PDB4V0 | SWITCH12 |
| H4 | IO114NDB4V0 | SWITCH2 |
| H2 | IO113PDB4V0 | SWITCH3 |
| E5 | IO125NDB4V0 | SWITCH5 |
| F4 | IO124NDB4V0 | SWITCH6 |
| J1 | IO112PPB4V0 | UART_CTS |
| P4 | IO96PDB4V0 | UART_DSR |
| P3 | IO101NDB4V0 | UART_DTR |
| N4 | IO100NPB4V0 | UART_RTS |
| M1 | IO103PDB4V0 | UART_RXD |
| N1 | IO103NDB4V0 | UART_TXD |

# 6 Board Stack-Up

The Fusion Advanced Development Kit board is built on a 10-layer printed circuit board (PCB). The top and bottom silkscreens are provided in Figure 39, page 36 and Figure 40, page 37. Full PCB design layout is provided in the Fusion Advanced Development Kit page. To view the PCB design layout files, you can use Allegro Free Physical Viewer, which can be downloaded from the Cadence website Allegro Download page: www.cadence.com/products/pcb/Pages/Downloads.aspx.

The layers are arranged in the following order:

- Layer 1: Top signal (Figure 39, page 36)
- Layer 2: GND1
- Layer 3: Sig1
- Layer 4: GND2
- Layer 5: PWR 1
- Layer 6: PWR 2
- Layer 7: GND3
- Layer 8: Signal 2
- Layer 9: GND 4
- Layer 10: Bottom signal (Figure 40, page 37)

***Figure 39 •*** **Layer 1, Top Silkscreen**

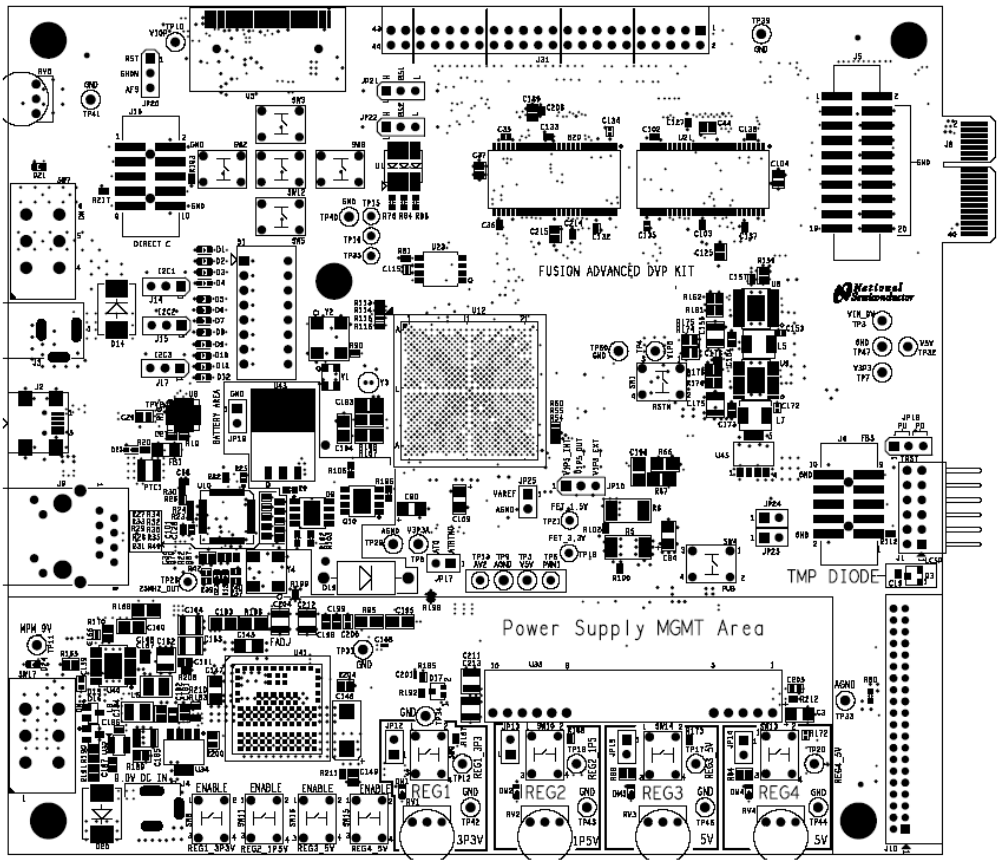
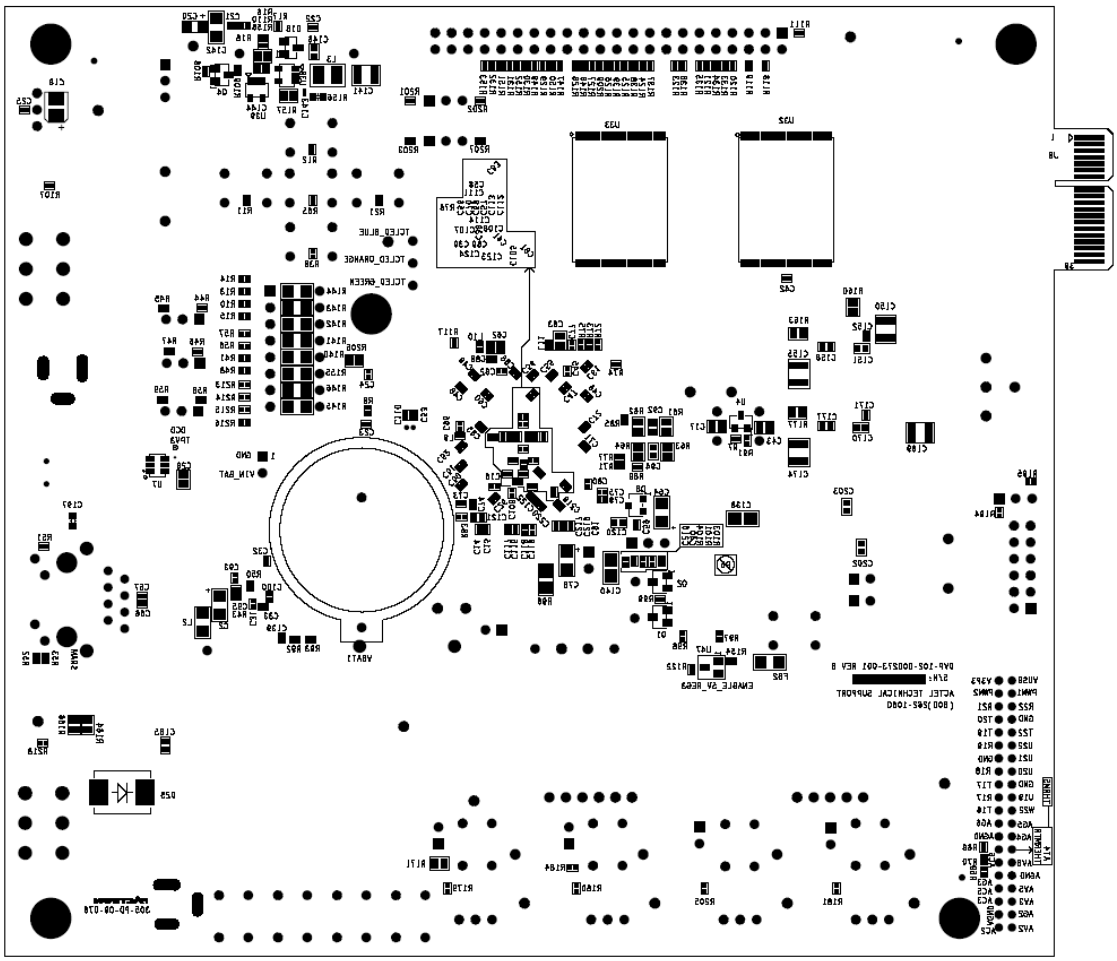


***Figure 40 •*** **Layer 10, Bottom Silkscreen**



# 7 Manufacturing Test

## 7.1 M1AFS-ADV-DEV-KIT Board Testing Procedures

This chapter defines and describes the specific M1AFS-ADV-DEV-KIT board testing procedures. Instructions for running the Microsemi M1AFS-ADV-DEV-KIT Board Tests are detailed. The steps needed to set up the test environment are also outlined. Associated files for this procedure can be downloaded at: http://soc.microsemi.com/download/rsc/?f=M1AFS_ADV_DEV_KIT_DF.

**Note:** The latest revision of Fusion Advanced Development Kit (M1AFS-ADV-DEV-KIT-PWR-2) has the same testing procedure as M1AFS-ADV-DEV-KIT.

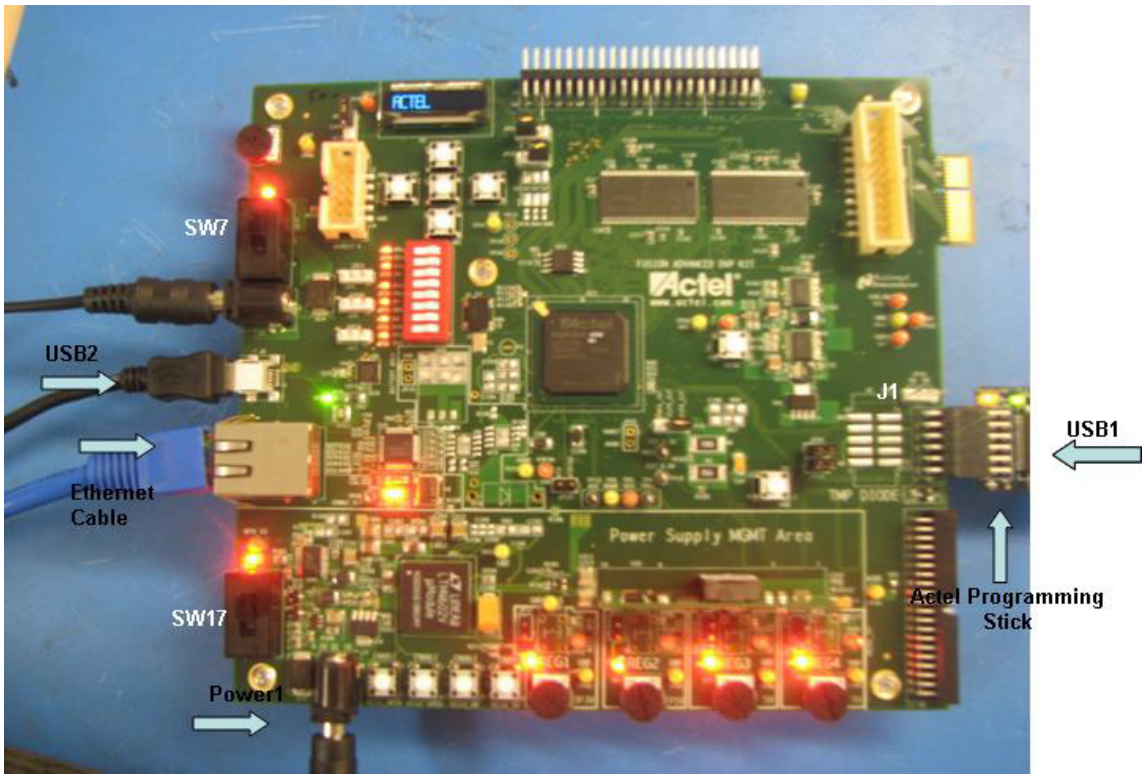
## 7.2 Installing the M1AFS-ADV-DEV-KIT Board USB Serial Driver

1. Use WinZip to extract all files stored in the `CP210x_Drivers.zip` archive.
2. Double-click on the file named `CP210x_Drivers.exe`.
3. Choose the **Install** option in the Install Wizard and select **Yes** for the licensing agreement.
4. Restart the computer on which the driver was installed. After restart, the driver can be used to communicate with the M1AFS-ADV-DEV-KIT board.

## 7.3 Hooking up the Board and Programming Stick

1. Connect the Microsemi M1AFS-ADV-DEV-KIT board to the Microsemi programming stick. Connect the J1 pins on the M1AFS-ADV-DEV-KIT board to the programmer, as shown in the following figure.

***Figure 41 •*** **Connect J1 Pins on M1AFS-ADV-DEV-KIT Board**




2. Connect one end of USB mini B cables to the USB connections on the M1AFS-ADV-DEV-KIT board and the Microsemi programming stick. These connections are labeled USB 1 and USB 2 in Figure 41, page 38.
3. Connect the USB cables to the PC you will use for testing.

4. Connect one end of a 9 V power supply to power input, Power1, on the M1AFS-ADV-DEV-KIT-PWR-2 board, as shown in Figure 41, page 38. Connect the end of another supply to input Power2. Plug both supplies into an electrical outlet.
5. When push-button SW15 is pressed after power-up, LED DM4 should light up.
6. Flip on power switch SW7 on the board. LEDs labeled D5 and D21 should light up. The LED labeled D3 on the programming stick should also be lighted.
7. Flip on power switch SW17 on the board. LEDs labeled DM1, DM2, DM3, and DM4 should light up.

## 7.4 Hooking Up the Board and Ethernet Cable

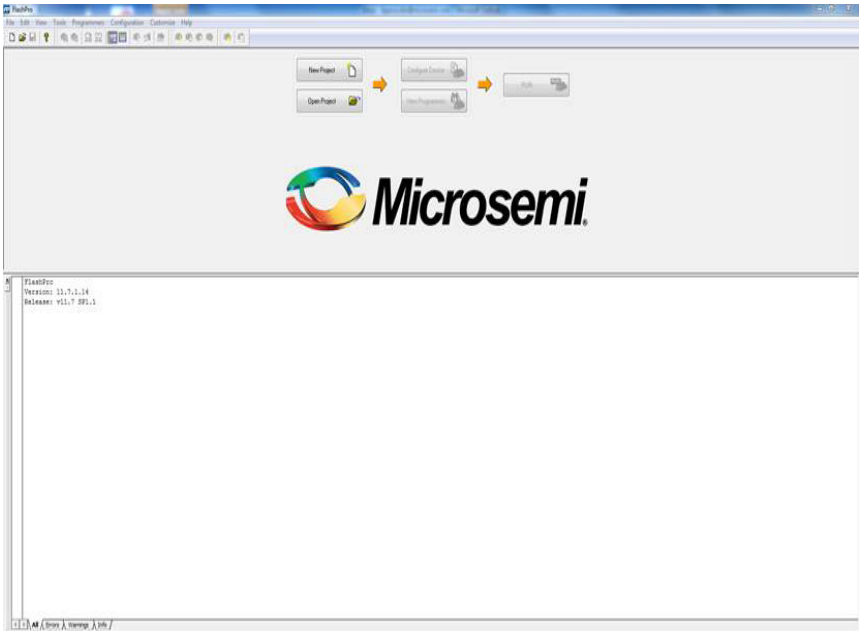
Connect an Ethernet cable from the local area network to J9, the M1AFS-ADV-DEV-KIT Ethernet jack.

**Note:** For the board Ethernet test to pass, the local network must be running a DHCP server that assigns an IP address to the web server on the board. Network firewalls must not block the board web server.

## 7.5 Programming the Board

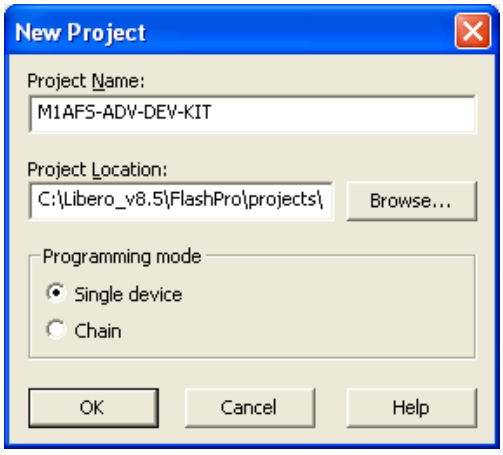
1. Open the FlashPro programming software.
2. Create a new programming project.

***Figure 42 •*** **New Project**



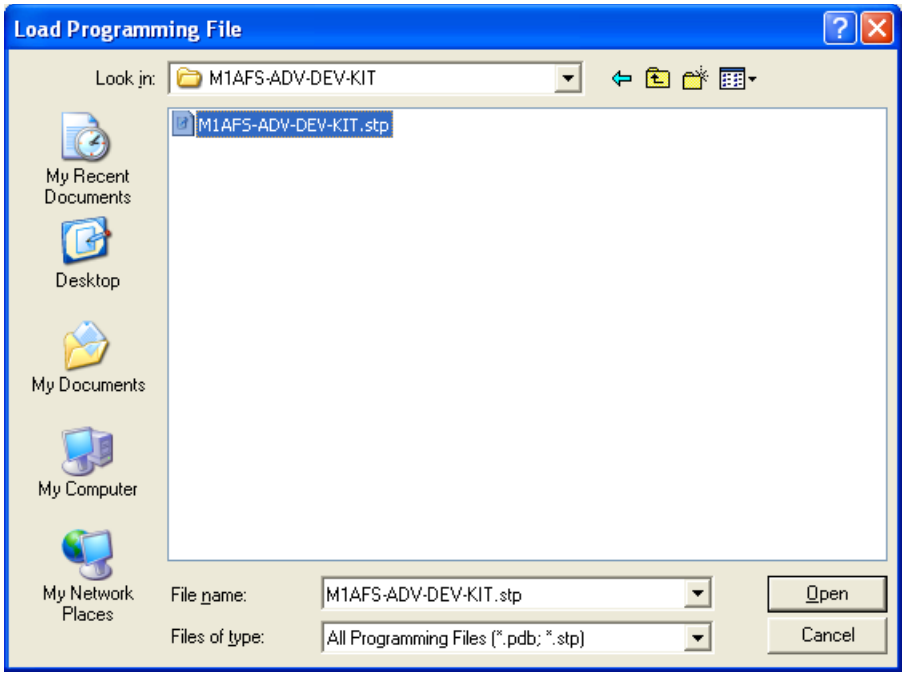

3. Select the option **Single Device** when choosing the programming mode.

***Figure 43 •*** **Select Single Device**



4. Click on the **Configure Device** button. This opens the Load Programming File window.
5. Browse the PC file system to find the M1AFS-ADV-DEV-KIT.stp programming file. Click **Open** to select the `M1AFS-ADV-DEV-KIT.stp` file.

***Figure 44 •*** **Load Programming File**

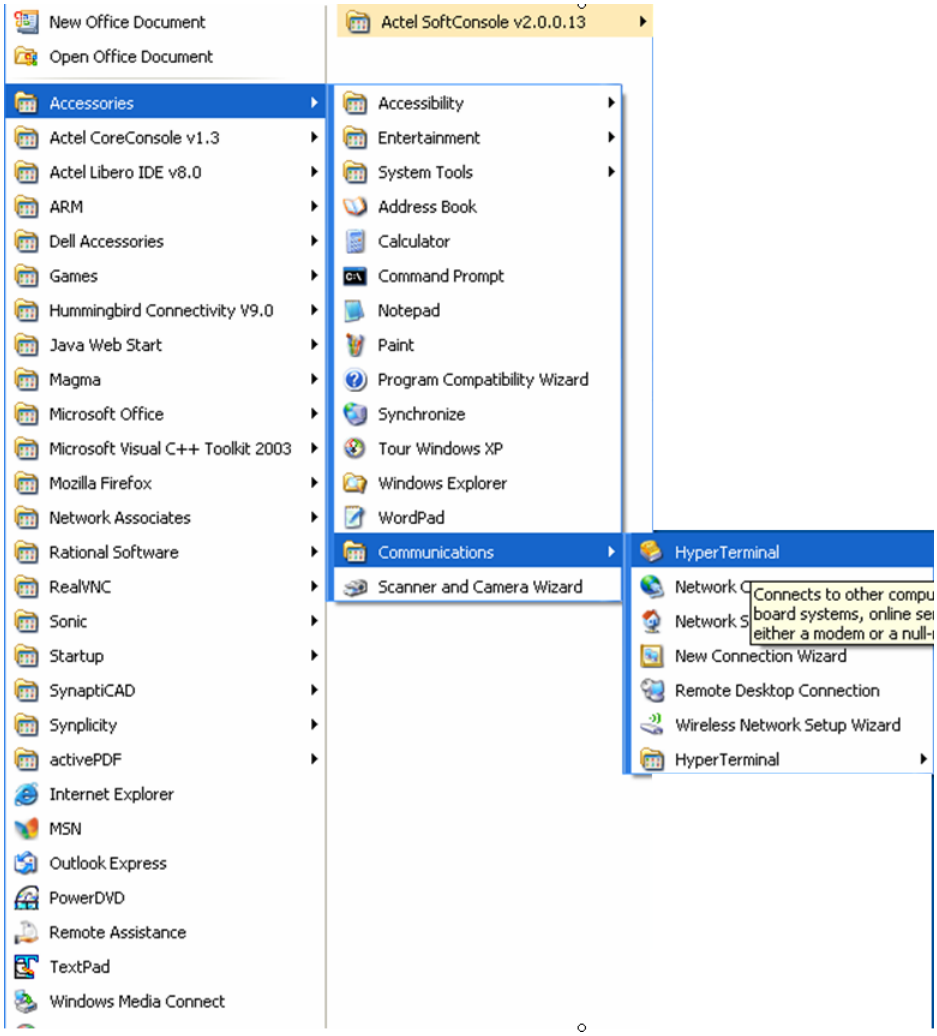



6. Click the **Program** button to program the M1AFS-ADV-DEV-KIT board.

## 7.6 Setting Up the Test Terminal

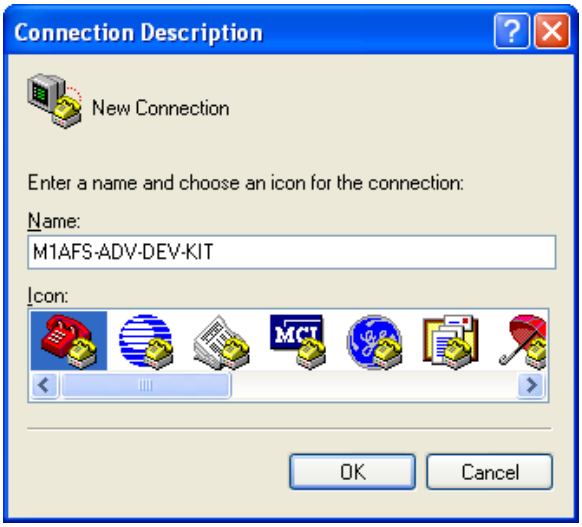
1. Open the Windows start menu. Select **All** > **Programs** > **Accessories** > **Communications** and select the **HyperTerminal** program. This opens HyperTerminal.

***Figure 45 •*** **Select HyperTerminal**



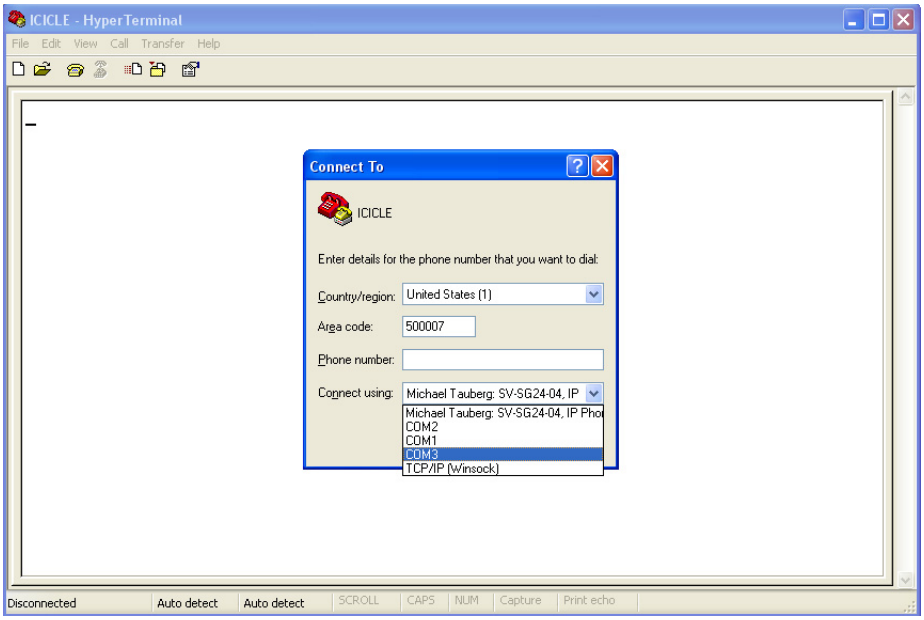
2. The **Connection Description** window will open. Type in **M1AFS-ADV-DEV-KIT** as the name of the new HyperTerminal session and click the **OK** button.

***Figure 46 •*** **Connection Description Window**



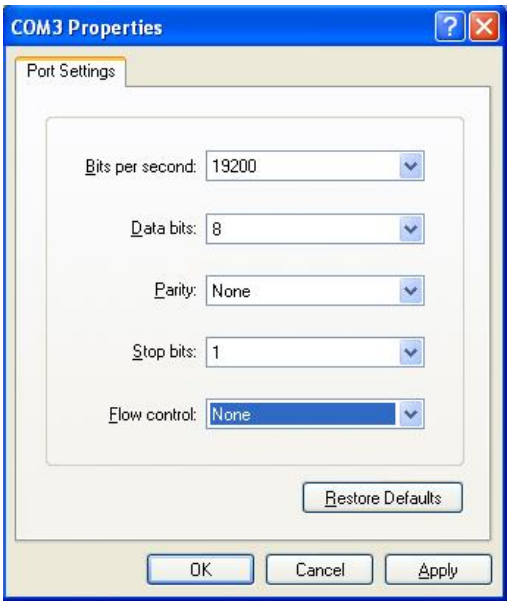

3. The Connect To window will open. Select the **COM3** serial connection.

***Figure 47 •*** **Select COM3 Serial Connection**




4. The COM3 Properties window appears. Select the following settings:
   Bits per second = 19200
   Data bits = 8
   Parity = None
   Stop bits = 1
   Flow Control = None

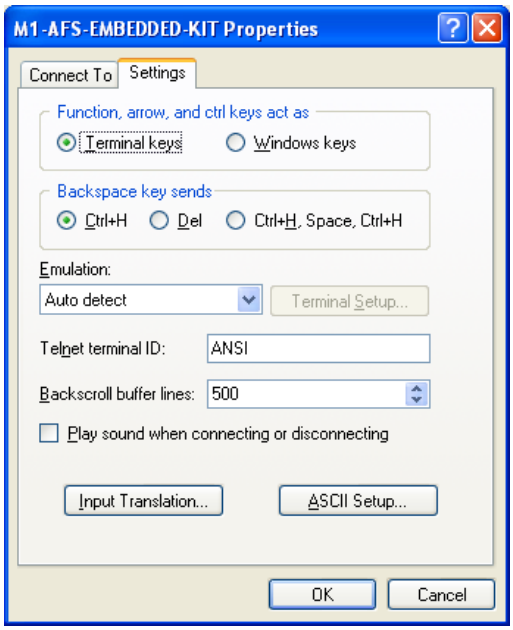
***Figure 48 •*** **COM3 Properties Window**




Click **OK** to keep the settings.

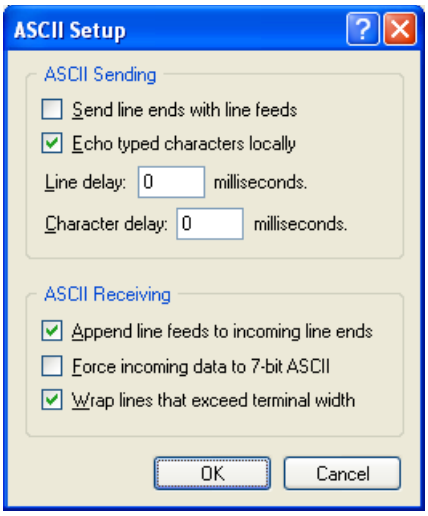
5. Select **File** >**Properties** in the HyperTerminal window. Choose the **Settings** tab.

***Figure 49 •*** **HyperTerminal Settings Tab**




6. Click the **ASCII Setup** button. Select the check box labeled **Append line feeds to incoming line ends**.

***Figure 50 •*** **ASCII Setup**



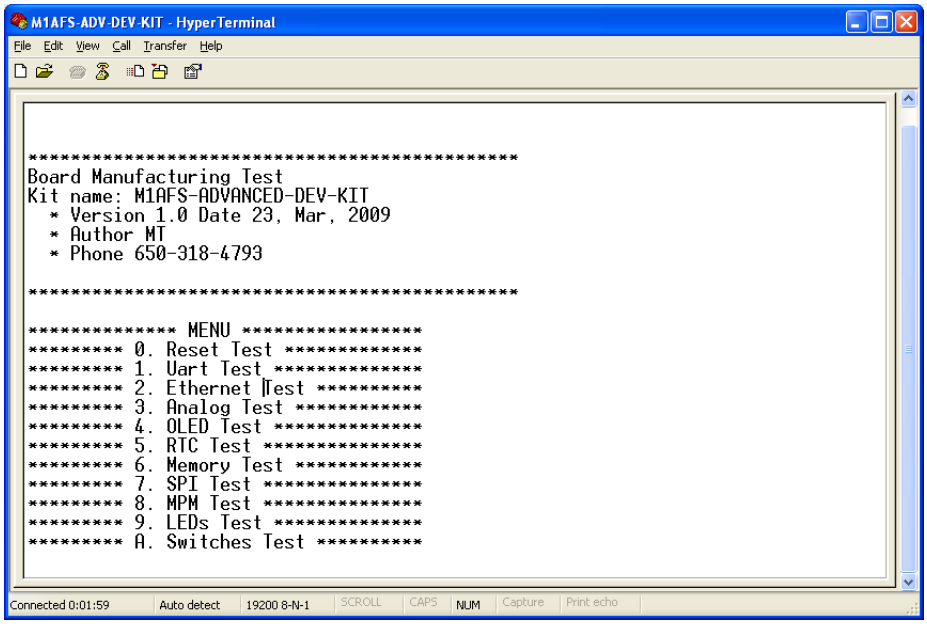

## 7.7 Running the M1AFS-ADV-DEV-KIT Board Test

**Note:** If the testing environment is not set up correctly, the M1AFS-ADV-DEV-KIT board test will not be possible. Ensure to complete Installing the M1AFS-ADV-DEV-KIT Board USB Serial Driver, page 38 through Programming the Board, page 39 correctly before beginning testing.

### 7.7.1 Procedure

1. Press the button labeled SW1 on the M1AFS-ADV-DEV-KIT board to start the test program.
2. The menu shown in the following figure appears on the terminal.

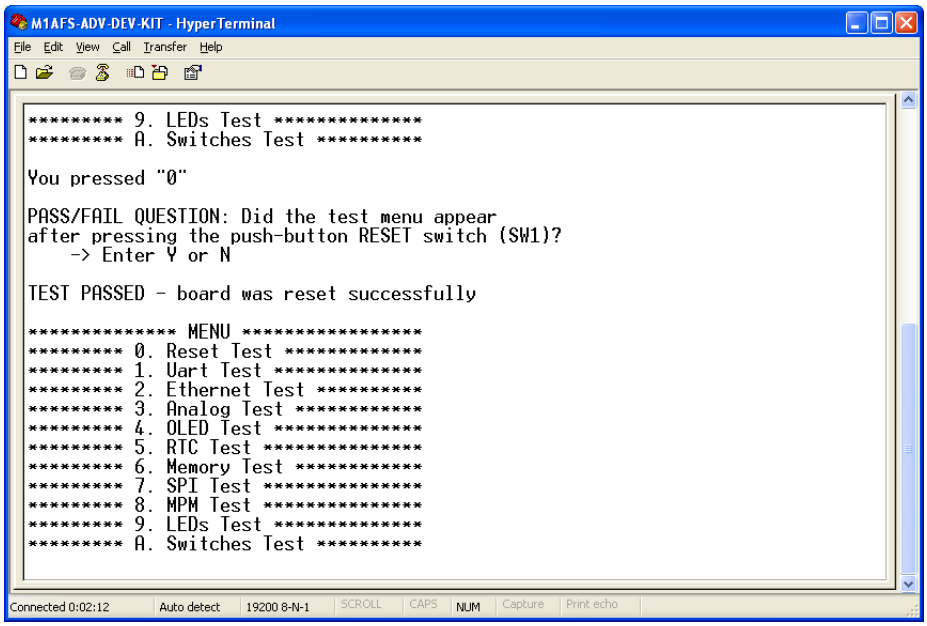
***Figure 51 •*** **HyperTerminal Menu**




If this message does not appear, try pressing button SW1 again. If the above message still does not appear, return to Programming the Board, page 39 and check to see that the terminal has been set up correctly.

3. Enter **0** into the terminal to begin the Reset Test.
   The message shown in the following figure should be displayed.

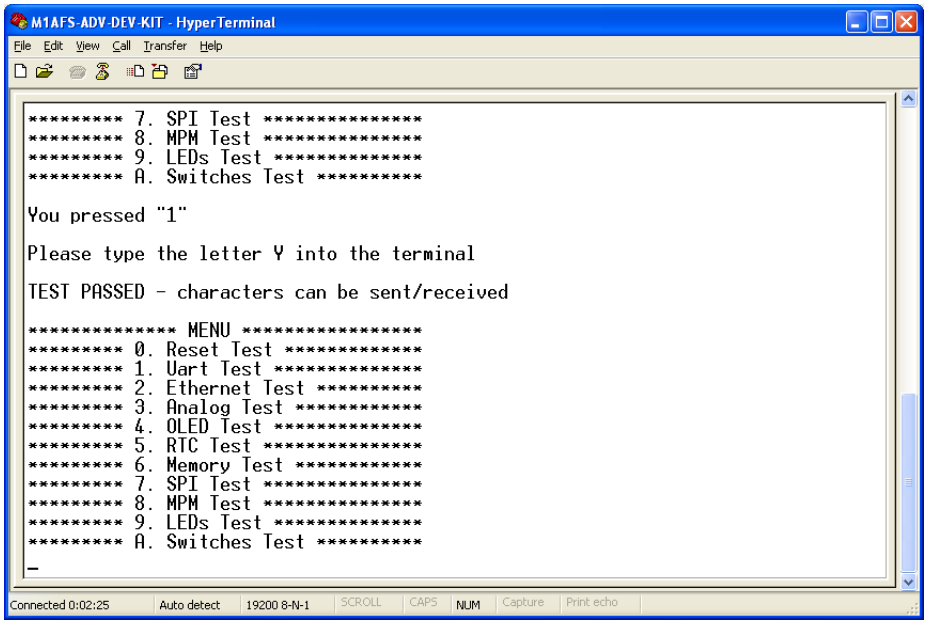
***Figure 52 •*** **Reset Test Passed**




If the menu appears correctly, enter the character **Y** into the terminal.

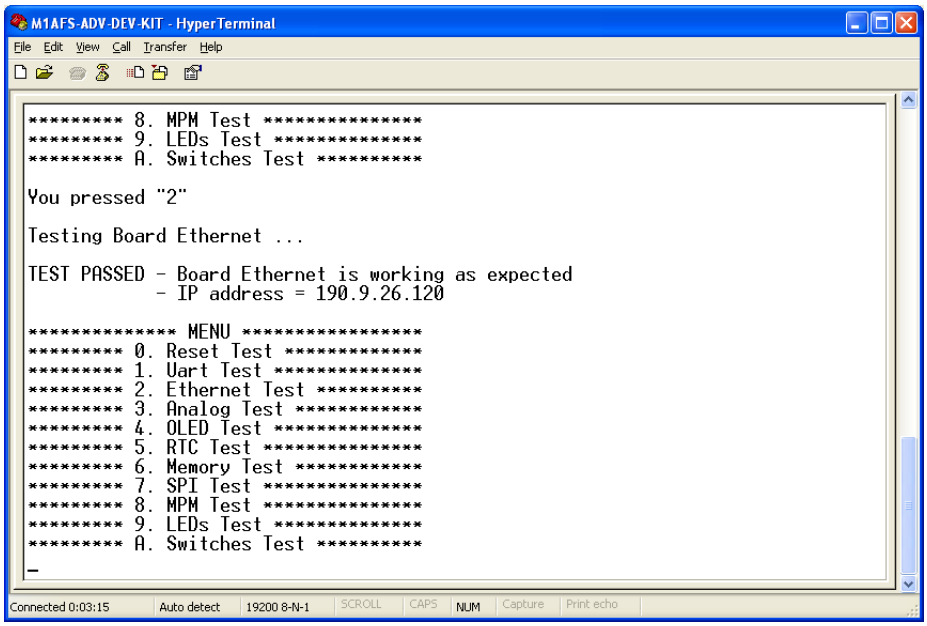
4. Enter **1** into the terminal to begin the UART test. Type the character **Y** into the terminal. The screen shown in the following figure should appear.

***Figure 53 •*** **UART Test Passed**



5. Enter **2** into the terminal to begin the Ethernet Test. The screen shown in the following figure should appear.

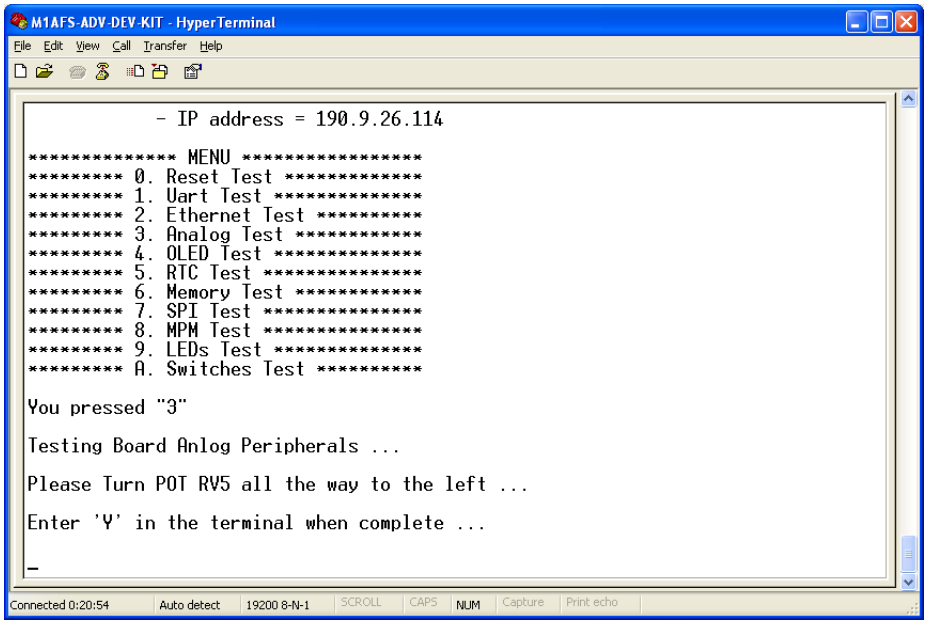
***Figure 54 •*** **Ethernet Test Passed**




**Note:** The IP address field need not be the same for the test to pass.

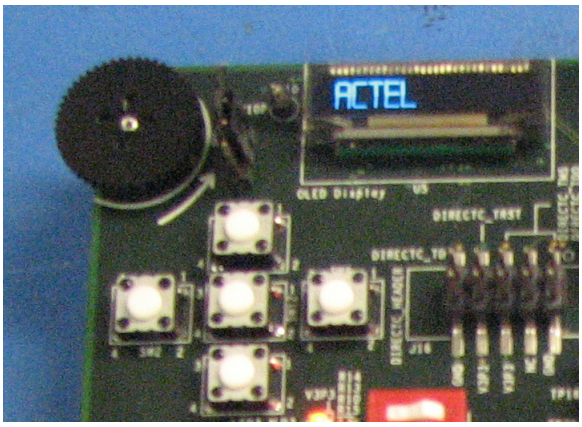
6. Enter **3** into the terminal to begin the Analog Test. The screen shown in the following figure should appear.

***Figure 55 •*** **Peripherals Test**



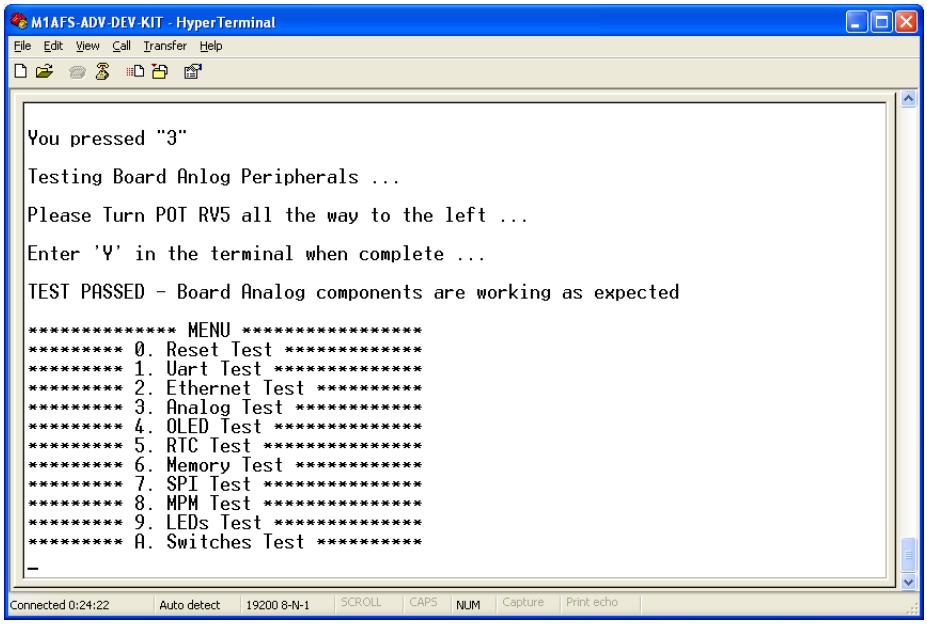
7. Locate POT RV5 on the top, left hand corner of the board. Turn POT RV5 counter-clockwise all the way to the left, as shown in the following figure.

***Figure 56 •*** **Turn POT RV5 Knob Counter-Clockwise**



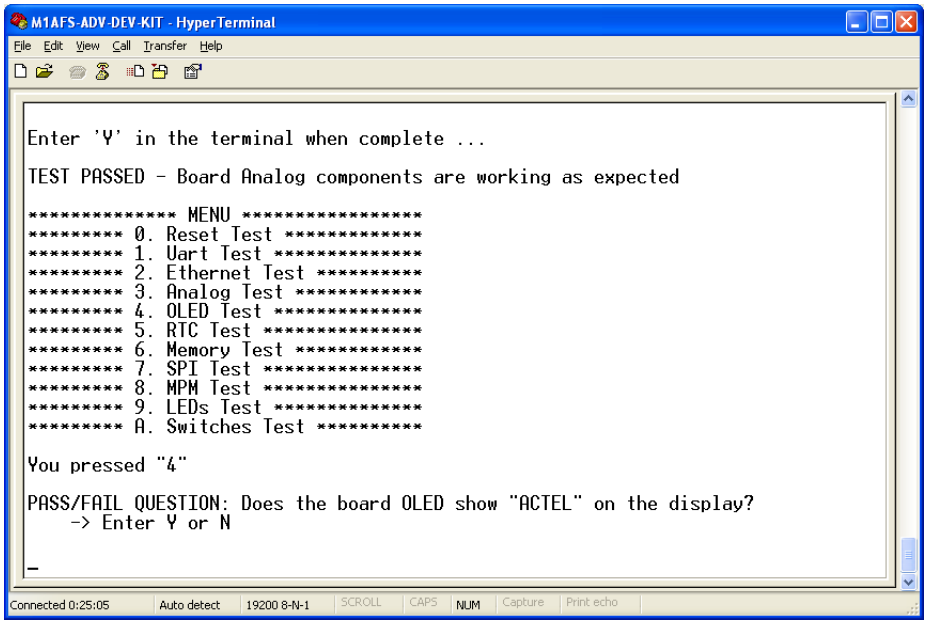

8. When done turning the POT, enter **Y** in the terminal. The screen shown in the following figure should appear.

***Figure 57 •*** **Analog Test Passed**



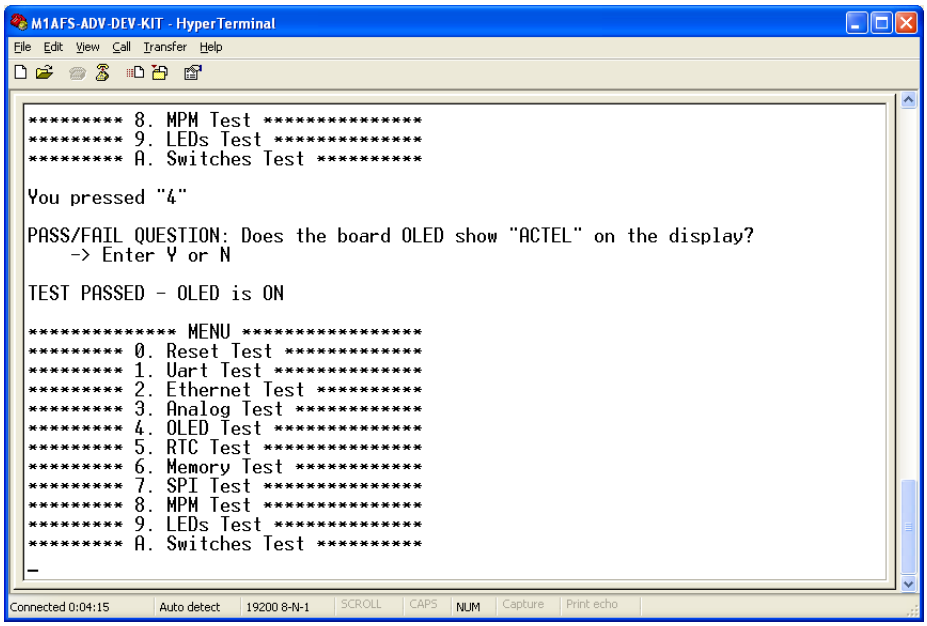
9. Enter **4** into the terminal to begin the OLED Test. The screen shown in the following figure appears.

***Figure 58 •*** **OLED Test**




10. Check the board OLED display. If the Character Microsemi is displayed in the OLED, enter **Y** in the terminal; otherwise, enter **N**. If Y was entered, the screen shown in the following figure will be displayed.

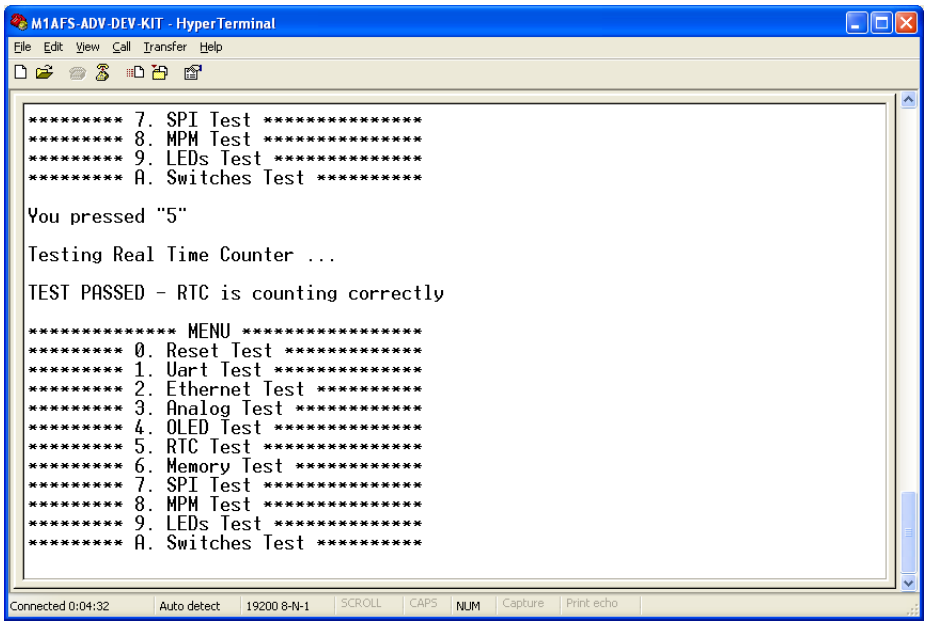
***Figure 59 •*** **OLED Test Passed**



11. Enter **5** into the terminal to begin the RTC Test. After a few seconds, the screen shown in the following figure should appear.

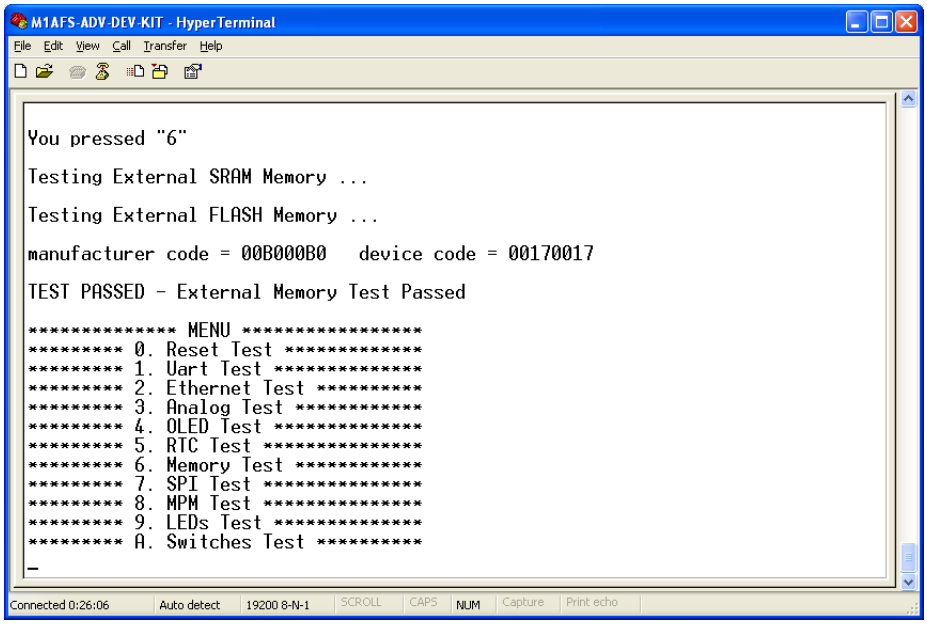
**Note:** The latest revision of Fusion Advanced development kit (M1AFS-ADV-DEV-KIT-PWR-2) does not contain OLED display on the board. You can skip this test.

***Figure 60 •*** **RTC Test Passed**



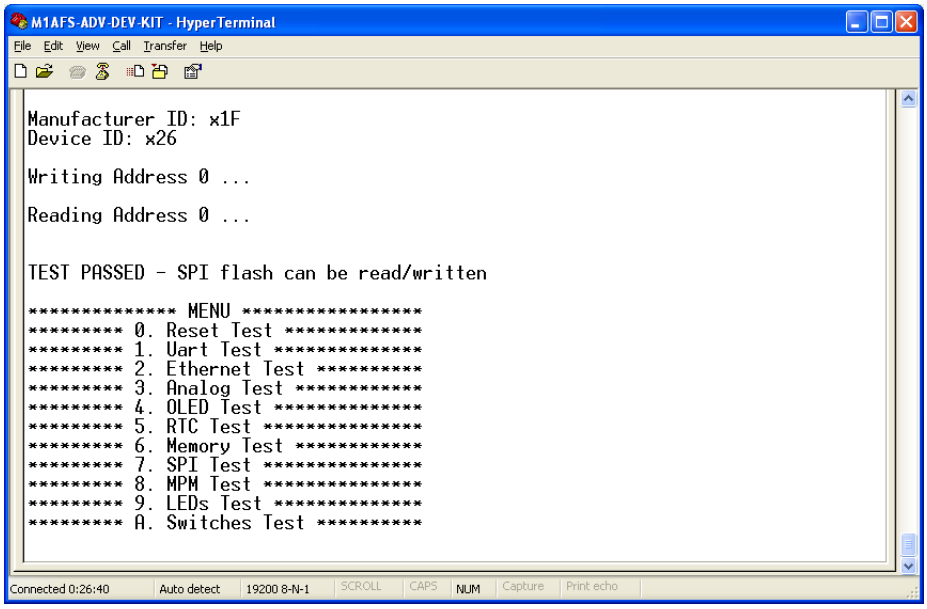

12. Enter **6** into the terminal to begin the Memory Test. After several seconds, the screen shown in the following figure should appear.

***Figure 61 •*** **Memory Test Passed**



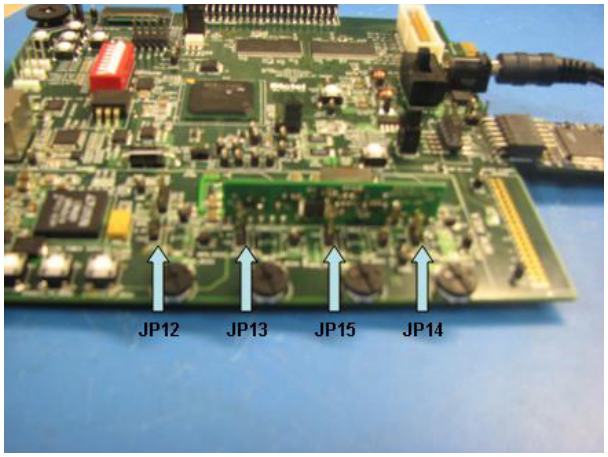
13. Enter **7** into the terminal to begin the SPI Test. The screen shown in the following figure will appear.

***Figure 62 •*** **SPI Test Passed**



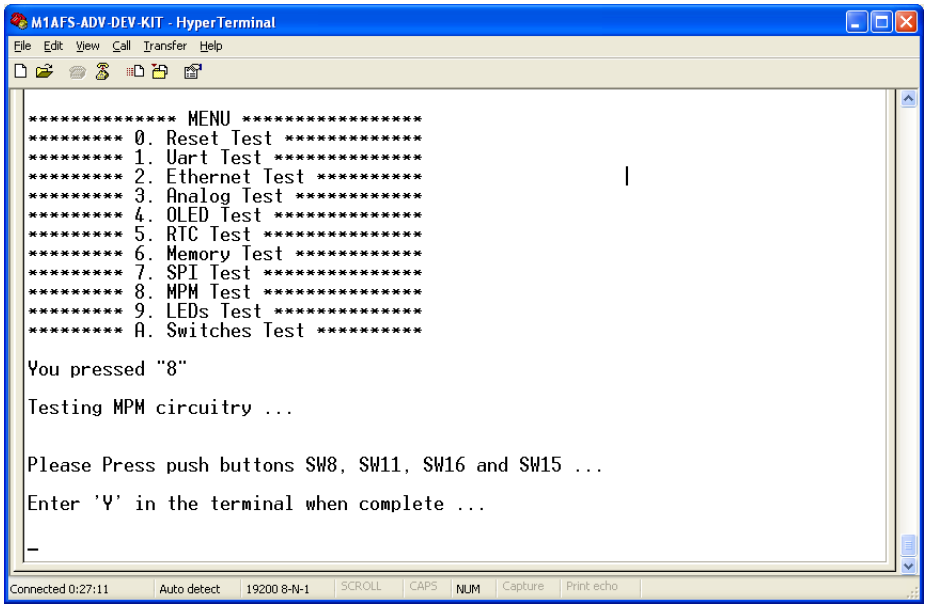

14. Remove jumpers JP12, JP13, JP14, and JP15 from the board, as shown in the following figure. Place the jumpers next to the board.

***Figure 63 •*** **Remove Jumpers J12 – J15**



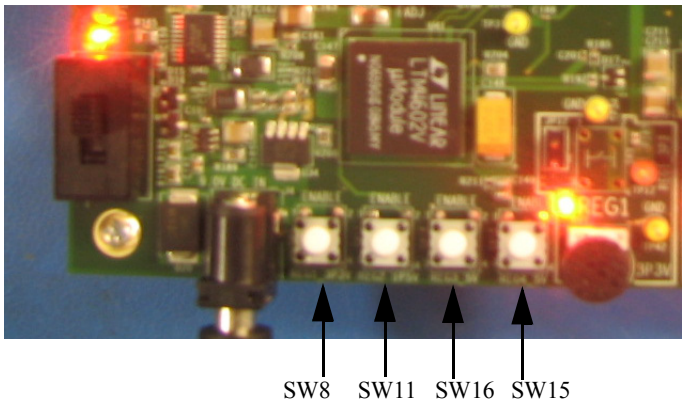
15. Enter **8** into the terminal to begin the MPM Test. The screen shown in the following figure will appear.

***Figure 64 •*** **MPM Test – Push-Buttons**



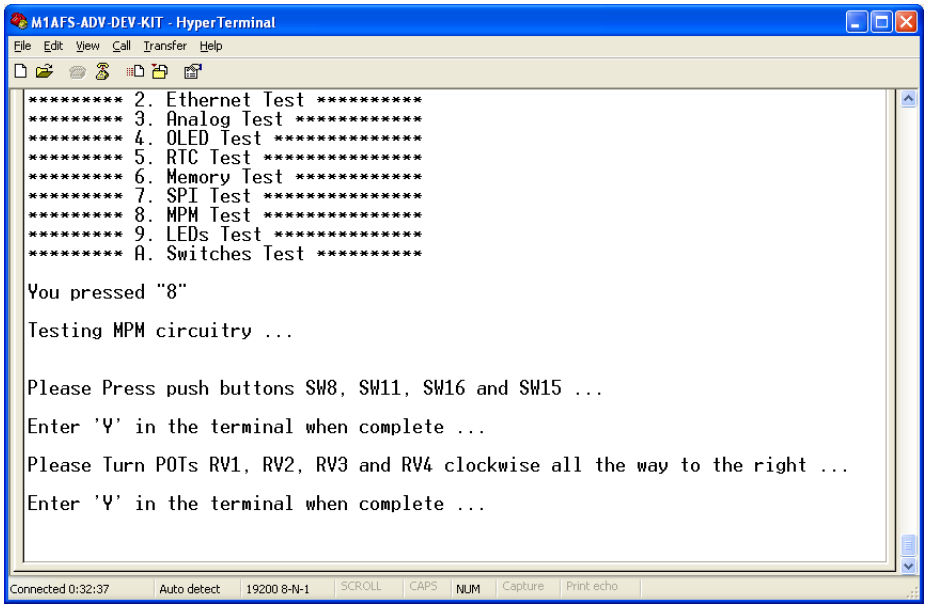

16. Press push-buttons SW8, SW1, SW16, and SW15, as shown in the following figure.

***Figure 65 •*** **Press Push-Buttons SW8, SW11, SW16, and SW15**



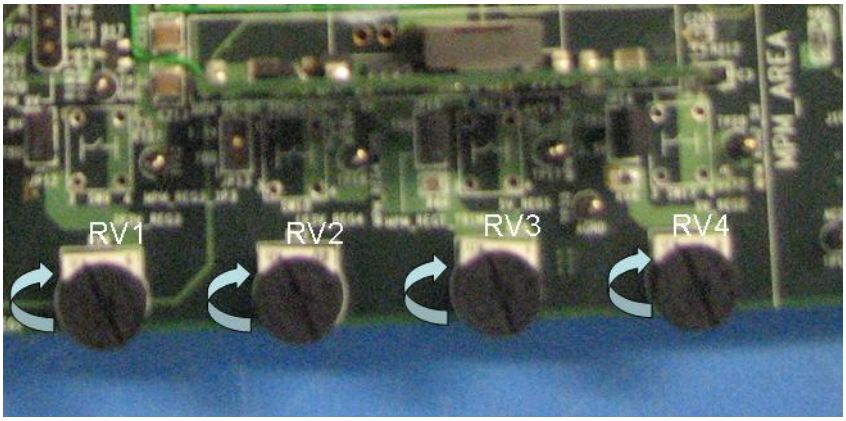
17. Enter **Y** in the terminal when complete. The screen shown in the following figure should appear.

***Figure 66 •*** **MPM Test – POTs**



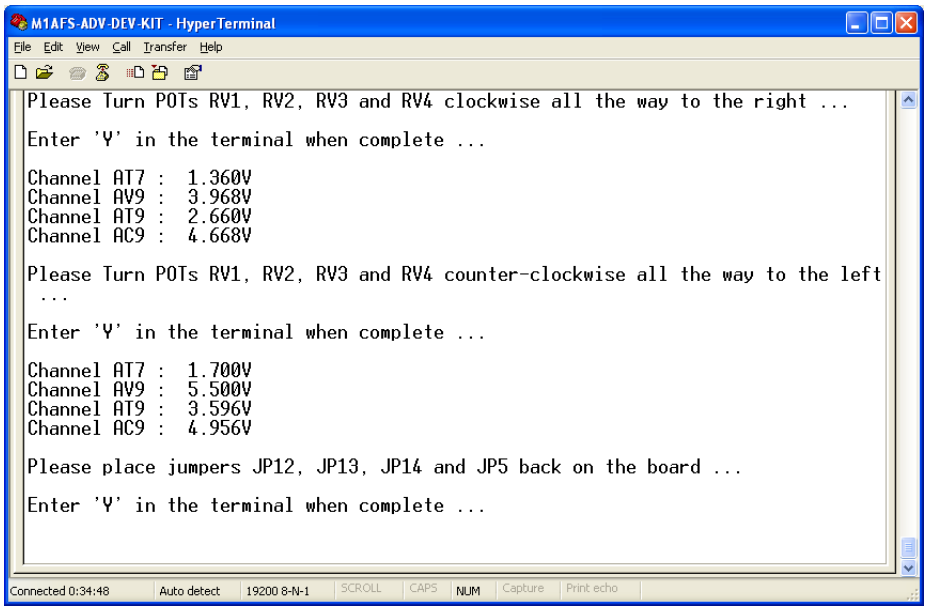

18. Turn POTs labeled RV1, RV2, RV3, and RV4 clockwise all the way to the right, as shown in the following figure.

***Figure 67 •*** **Turn POTs RV1 – RV4 Clockwise**



19. Enter **Y** in the terminal when done turning the POTs. The terminal screen shown in the following figure should appear.

***Figure 68 •*** **MPM Test – Replace Jumpers**




The voltages measured on the MPM rails will be printed out. They should be in the following range:

Channel AT7: 1.2 V – 1.4 V

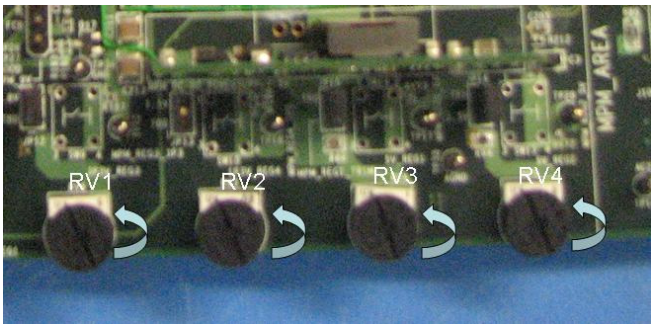
Channel AV9: 3.8 V – 4.1 V

Channel AT9: 2.5 V – 2.8 V

Channel AC9: 4.4 V – 4.7 V

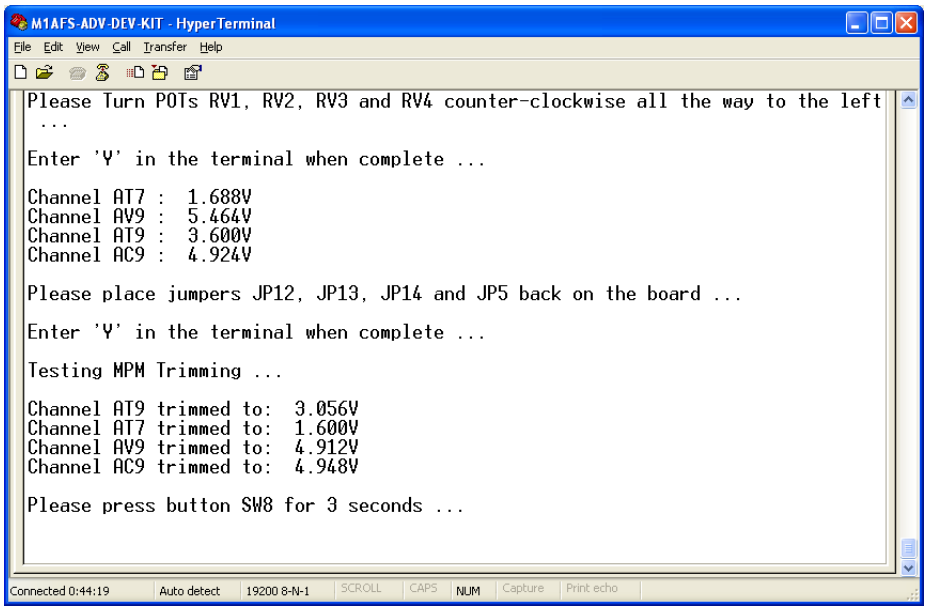
20. Turn POTs labeled RV1, RV2, RV3, and RV4 counter-clockwise all the way to the left, as shown in the following figure.

***Figure 69 •*** **Turn POTs RV1 – RV4 Counter-Clockwise**



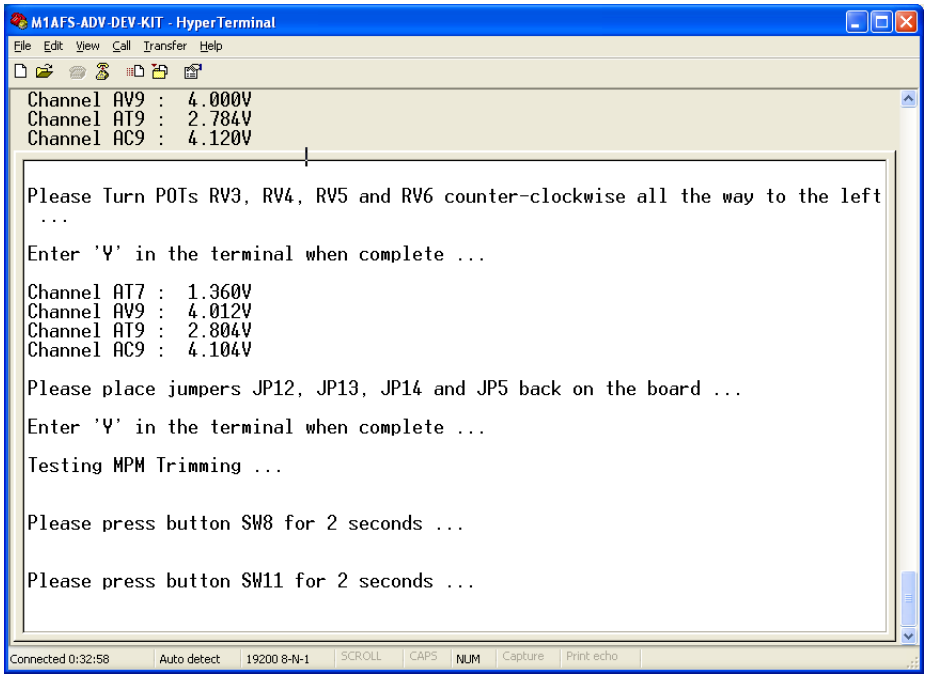
21. Enter **Y** in the terminal when done turning POTs. The terminal screen shown in the following figure should appear.

***Figure 70 •*** **MPM Test – Trimming**



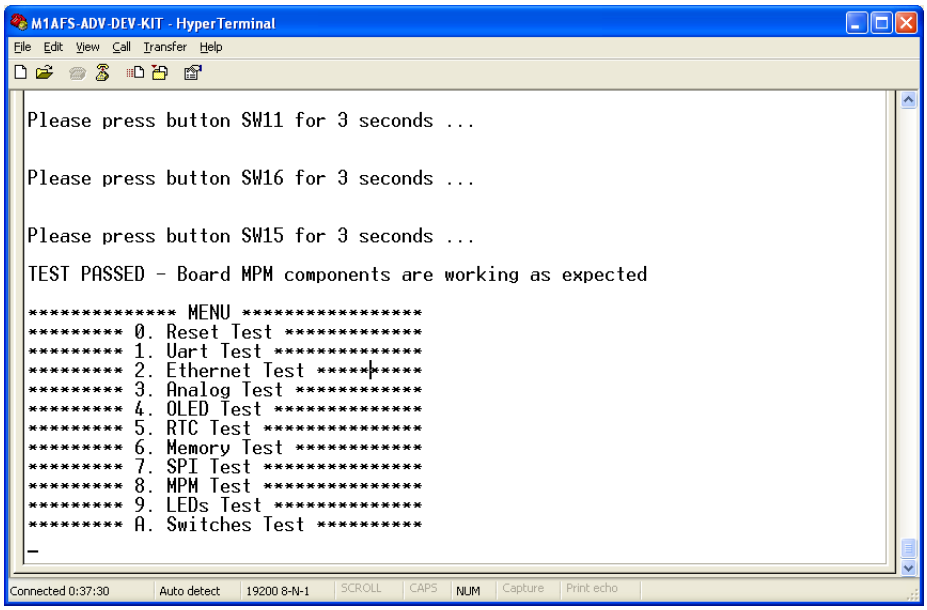

22. Press and hold push-button SW8 for 2 seconds. The screen shown in the following figure should appear.

***Figure 71 •*** **MPM Test – Trimming, Continued**



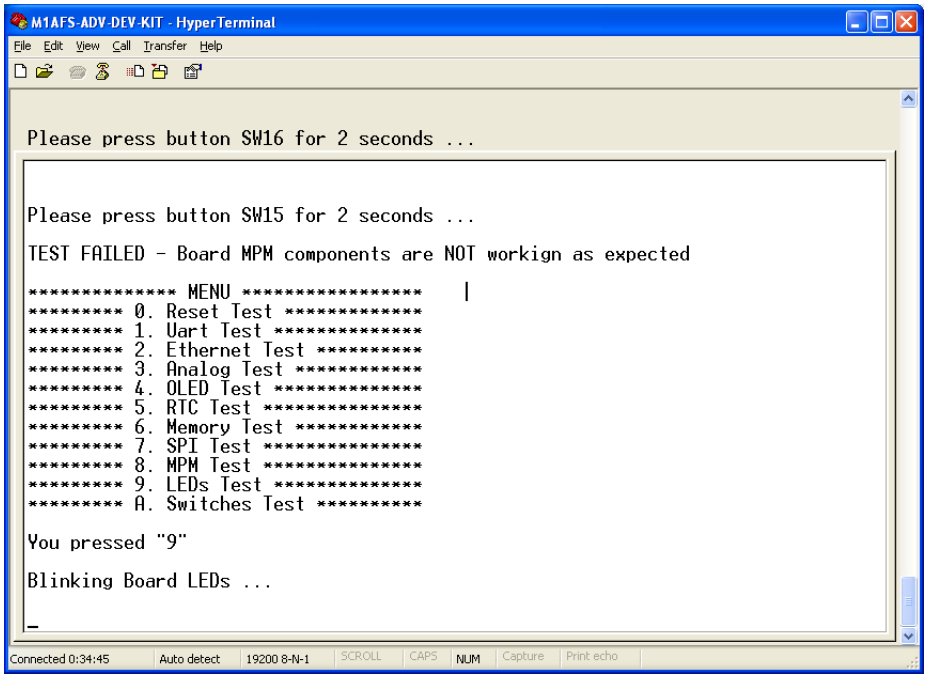
23. Repeat for the other push-buttons.
    When complete, the screen shown in the following figure should appear.

***Figure 72 •*** **MPM Test Passed**



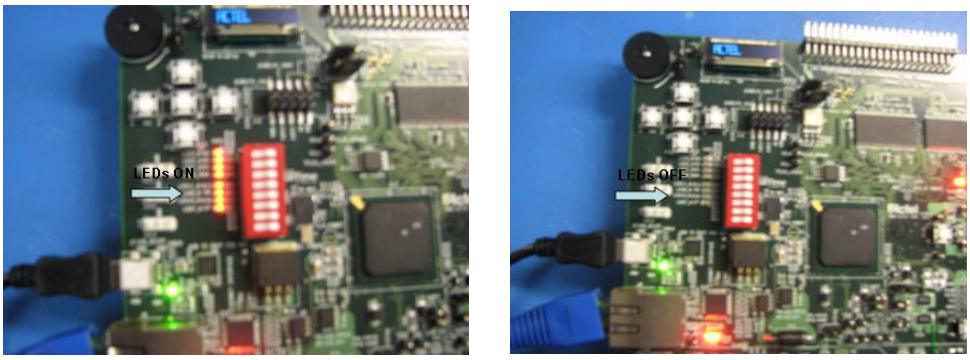

24. Enter **9** into the terminal to begin the LEDs Test. The screen shown in the following figure will appear.

***Figure 73 •*** **LEDs Test**



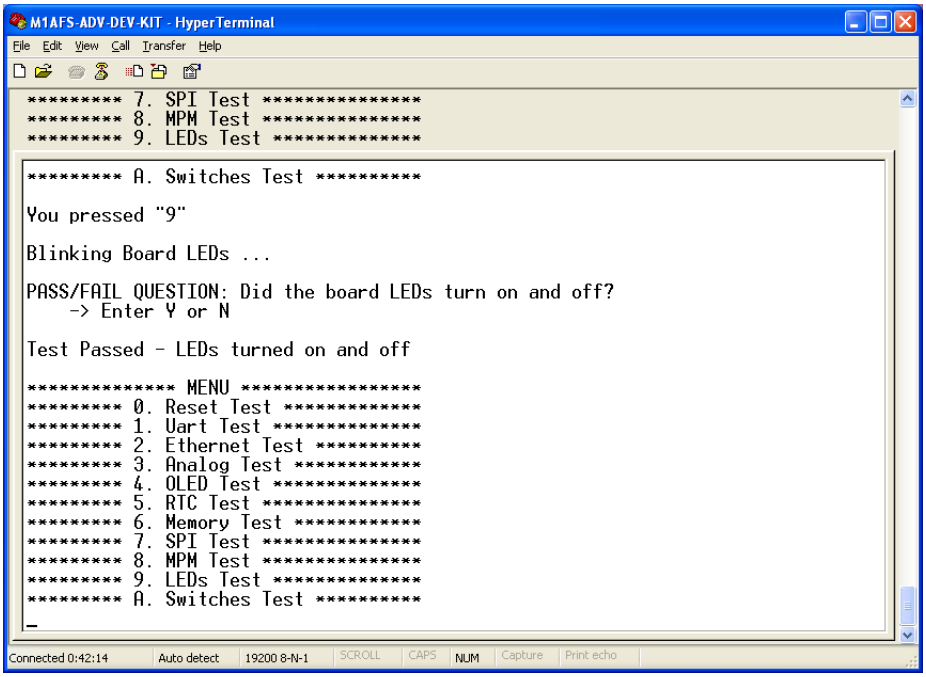
Board LEDs labeled D1, D2, D3, D4, D7, D9, D10, and D11 will blink on and off, as shown in the following figure.

***Figure 74 •*** **LEDs On (left) and LEDs Off (right)**



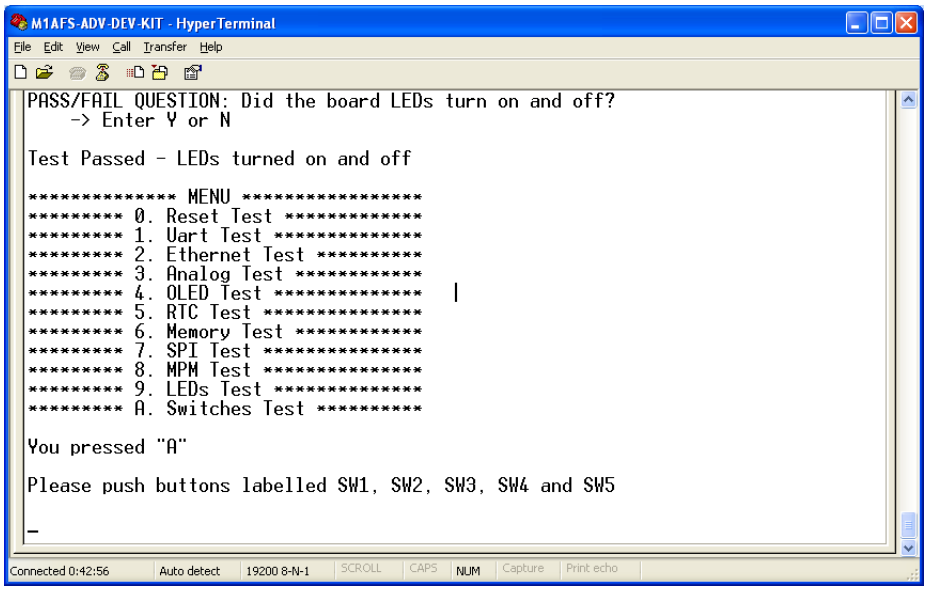

25. If you do observe the LEDs blinking, enter **Y** in the terminal. Otherwise enter **N**. If Y was entered, the screen shown in the following figure will be displayed.

***Figure 75 •*** **LEDs Test Passed**



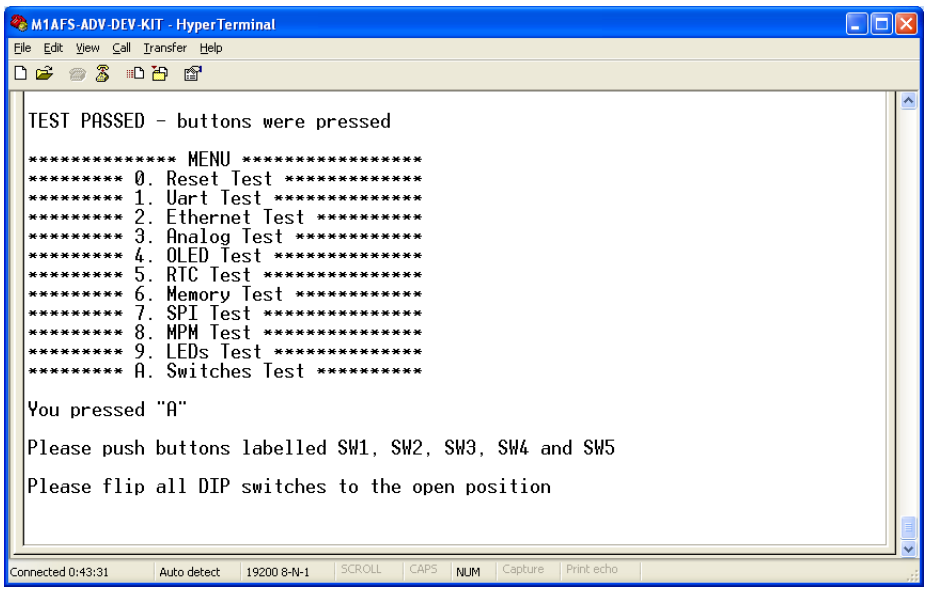
26. Enter **A** into the terminal to begin the Switches Test. The screen shown in the following figure will appear.

***Figure 76 •*** **Begin Switches Test**



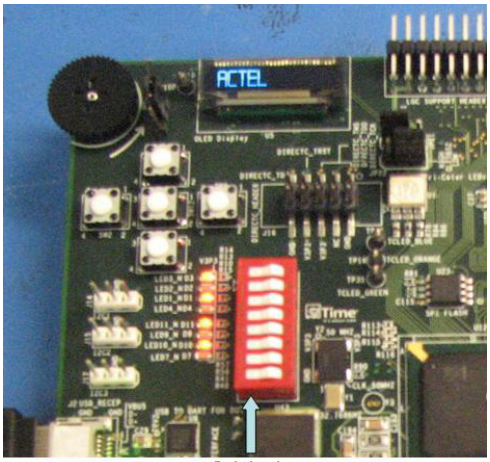

27. Press switches on the board labeled SW1, SW2, SW3, SW4, and SW5. After all switches have been pressed, the screen shown in the following figure should be displayed.

***Figure 77 •*** **Switches Test – DIP Switches**



28. Flip all DIP switches on the board to the OPEN position, as shown in the following figure.

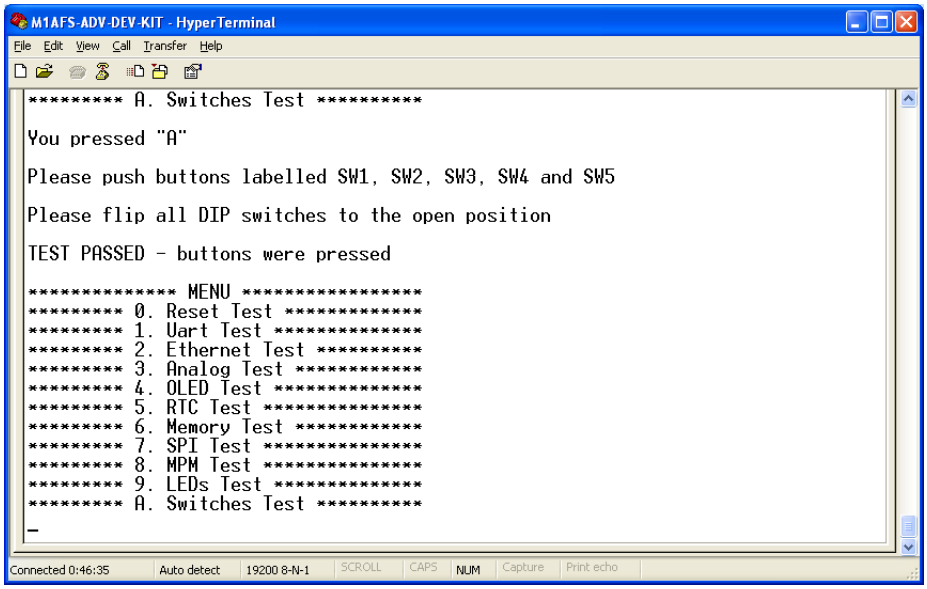
***Figure 78 •*** **DIP Switches Open**




Switches in
"OPEN" position

The screen shown in the following figure should appear after the switches have been flipped.

***Figure 79 •*** **Switches Test Passed**




# 7.8 M1AFS-ADV-DEV-KIT Board Failures

All Tests outlined in Running the M1AFS-ADV-DEV-KIT Board Test, page 44 should result in the words "TEST PASSED" being printed on the terminal. If this does not happen, or the words "TEST FAILED" are printed, the test has failed.

If the M1AFS-ADV-DEV-KIT board fails any of the tests outlined in Running the M1AFS-ADV-DEV-KIT Board Test, page 44, the board being tested is not functional.